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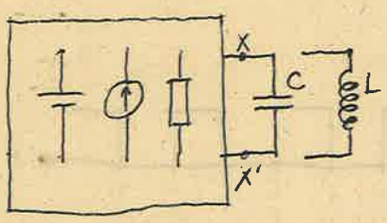
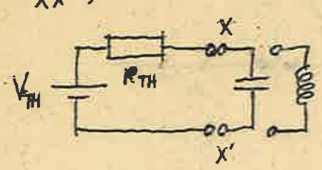
LINEAR WAVESHAPING

Networks containing single energy storage elements
(Sources are constant)



Statement : All the waveforms in such a network will be either exponential or constant

Proof : Find Thevenin equivalent circuit across xx' :



$$C\frac{dV_c}{dt} = \frac{1}{R_{TH}}(V_{TH} - V_c)$$

$$V_c(t) = k_1 + k_2 e^{-t/\tau}$$

$$\tau = R_{TH}C$$

To find any waveform, apply superposition (After finding V_c, Capacitor is replaced by a voltage source V_c) :

$$y(t) = k_1' + k_2' + k_3' e^{-t/\tau}$$
$$= k_4 + k_3' e^{-t/\tau}$$

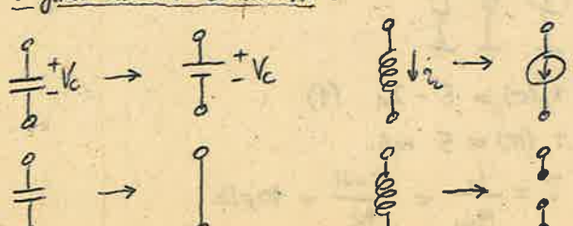
$$k_4 = y(\infty)$$
$$k_3' = y(0) - k_4$$

or

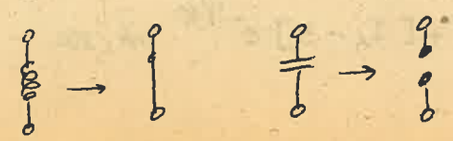
$$\boxed{y(t) = y(\infty) + [y(0) - y(\infty)]e^{-t/\tau}}$$

To find initial conditions :

at time $t=0$



at time $t=\infty$



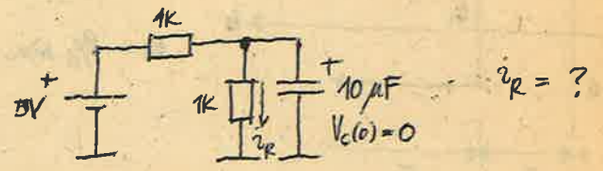
To find time constant (τ) :

Remove C (or L), short circuit voltage sources, open circuit current sources.
Find resistance across xx' (R_{TH})

$$\tau = R_{TH}C$$

$$\tau = \frac{L}{R_{TH}}$$

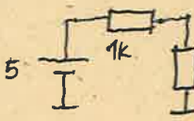
Example :



(1) Find initial value :

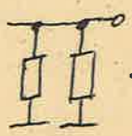
$$i_R(0) = 0$$

(2) Find the steady state value :



$$i_R(\infty) = 2.5\ mA.$$

(3) τ :

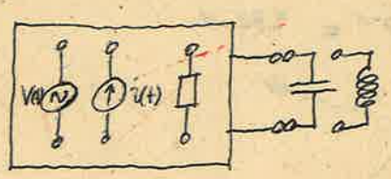


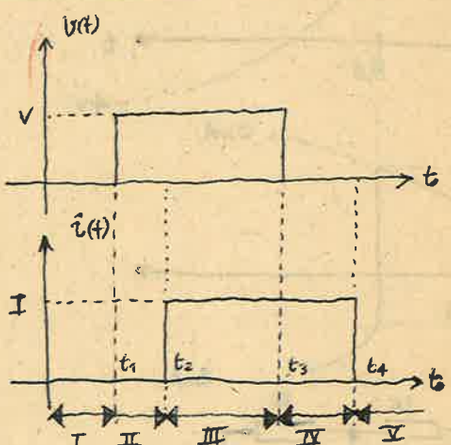
$R_{TH} = 0.5\ K$

$$\tau = (0.5K)(10\mu F) = 5\ mSec$$

$$i_R(t) = 2.5 + [-2.5]e^{-t/5}\ mA, mSec.$$

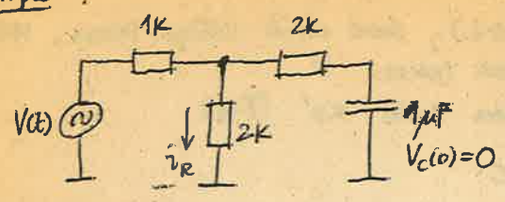
Networks containing pulse type sources :



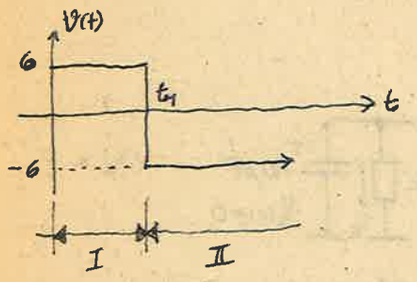


In each segments, Sources are constant; all the waveforms are exponential. Solve any waveform you are interested, and also $V_c(t)$, (or $i_L(t)$).
$V_c(t_1)$ is the initial state for region II
$V_c(t_2)$ " " " " " " III
⋮
$V_c(t_4)$ " " " " " " V

Example :

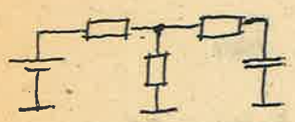


Find $i_R(t)$ for $t \geq 0$



$t_1 = 8/3$ msec.

Region (I) : $0 \leq t \leq t_1$ $v(t) = 6$ V



$i_R(0) = 1.5$ mA $\quad V_c(0) = 0$

$i_R(\infty) = 2$ mA $\quad V_c(\infty) = 4$ V.

$\tau = 8/3$ mSec.

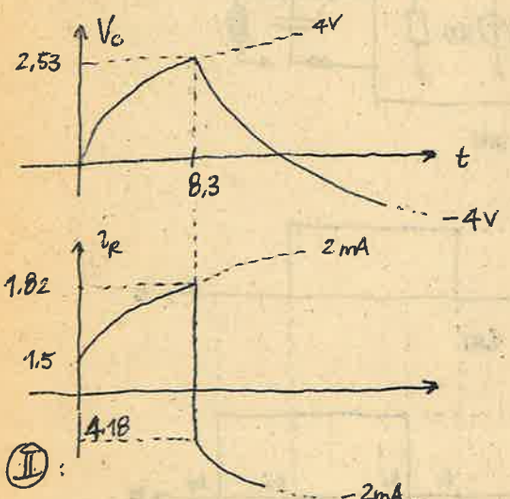
$(R_{TH} = 2K + (1K \| 2K)) = 8/3$ K.

$i_R(t) = 2 - 0.5\, e^{-t/8/3}$ mA, mSec.

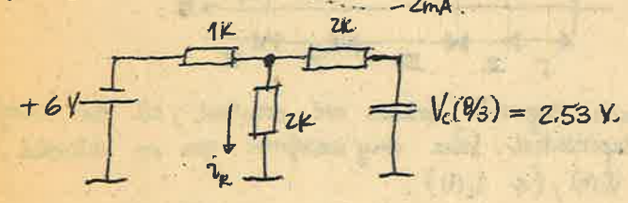
$v_c(t) = 4 - 4\, e^{-t/8/3}$ V, msec.

$V_c(8/3)_{msec} = 4 - 4e^{-1} = 2.53$ V.

$i_R(8/3) = 2 - 0.5e^{-1} = 1.82$ V.



Region (II) :



initial Values :

$$i_R(8/3^+)_{msec} = -\frac{6}{4} + \frac{2.53}{2+2/3} \cdot \frac{1}{3}$$

$$= -1.5 + \frac{2.53}{8} = -1.18 \text{ mA.}$$

$i_R(\infty) = -2$ mA $\quad V_c(\infty) = -4$ V

$i_R(t) = -2 + 0.72\, e^{-(t-8/3)/8/3}$ mA, mS.

$V_c(t) = -4 + 6.53\, e^{-(t-8/3)/8/3}$ V, mS.

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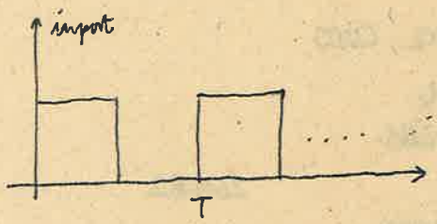
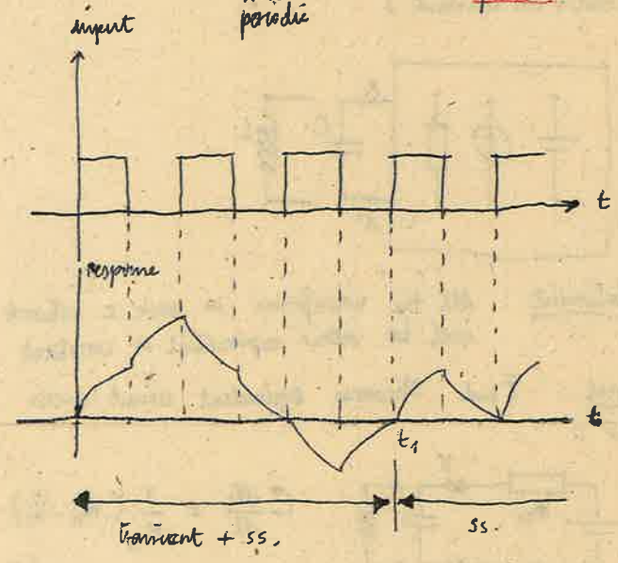
Response to periodic inputs

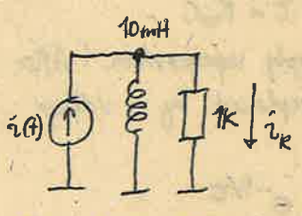


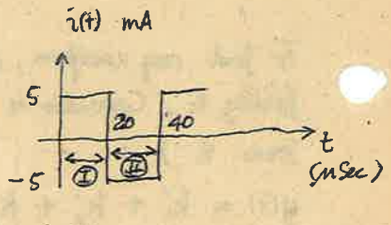
response = transient term + steady state term

(transient term: non periodic; steady state term: periodic)



Example :





Find steady-state $i_L(t)$, $i_R(t)$

Assume the circuit is at s.s at $t=0$

Assume $i_L(0) \triangleq I_A$

Take region (I)

$i_R(0) = 5 - I_A$ (1)

$i_L(\infty) = 5$ mA.

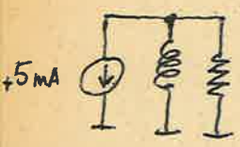
$\tau = \frac{L}{R_{TH}} = \frac{10\text{ mH}}{1K} = 10\,\mu\text{Sec.}$

$i_L(t) = 5 + [I_A - 5]\, e^{-t/10}$ mA, μsec.

$i_L(20^-\mu sec) = 5 + [I_A - 5]e^{-2} \triangleq I_B$ (2)

$i_R(20^-\mu sec) = 5 - I_B$ (3)

Region II



$i_L(20^+\mu sec) = I_B$

$i_R(20^+\mu sec) = -5 - I_B$ (4)

$i_L(\infty) = -5\ mA.$

$i_L(t) = -5 + [I_B + 5]e^{-(t-20)/10}$ mA, μsec.

$i_L(40^-\mu sec) = -5 + [I_B + 5]e^{-2} = I_A$ (5)

$i_R(40^-\mu sec) = -5 - I_A$ (6)

From (2) and (5) solve I_A and I_B :

$I_A = -6.15$ mA.

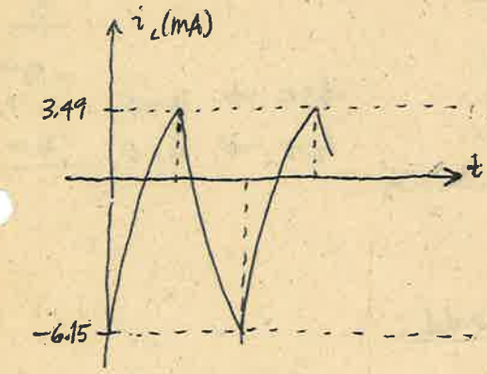
$I_B = 3.49$ mA.

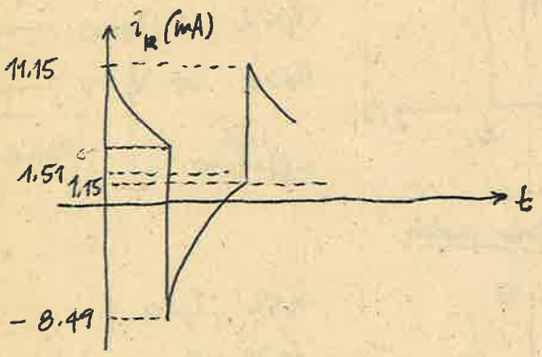
From (1) $i_R(0) = 11.15$ mA.

$i_R(20^-) = 1.51$ mA. (From 3)

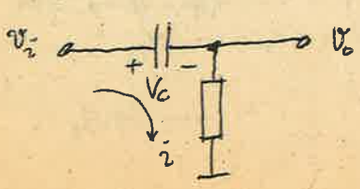
From (4) $i_R(20^+) = -8.49$ mA.

From (6) $i_R(40\ \mu sec) = 1.15$ mA.



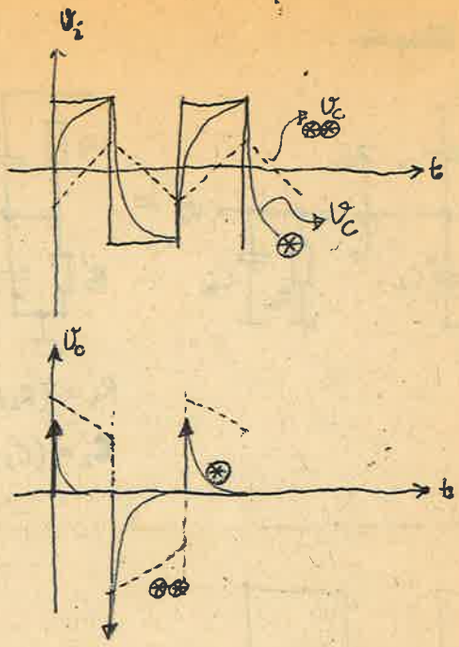


Differentiator :



$v_o = iR = RC\frac{d}{dt}(v_i - v_o)$

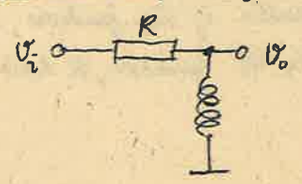
if $v_o \ll v_i \Rightarrow v_o = RC\frac{d}{dt}v_i$



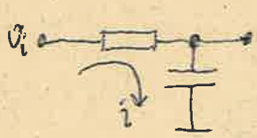
if $\tau \ll T$: ⊛

if $\tau \gg T$: ⊛⊛

differentiator by using inductor :



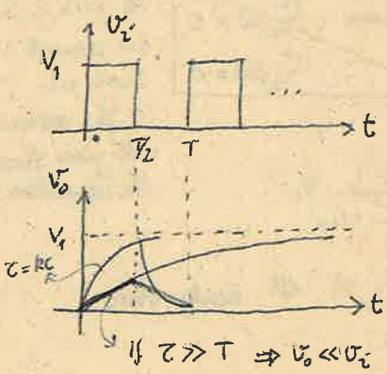
Integrator : 050382



$v_o = \frac{1}{C}\int i\,dt$

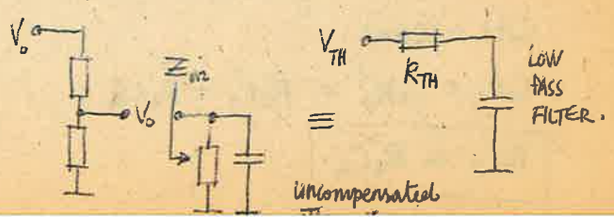
$= \frac{1}{CR}\int (v_i - v_o)\,dt$

if $v_o \ll v_i \Rightarrow v_o \cong \frac{1}{RC}\int v_i\,dt$

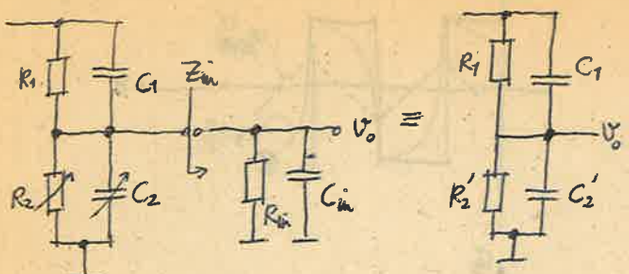


Compensated attenuator :

To decrease the amplitude of a signal without distorting the waveshape.

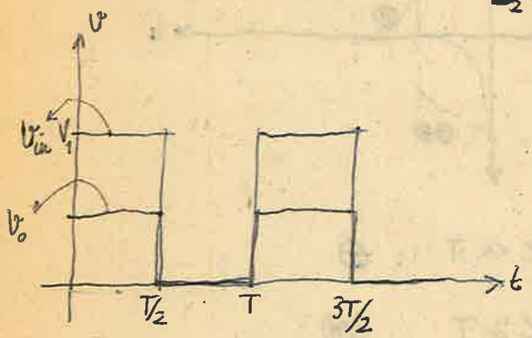


Compensated attenuator :



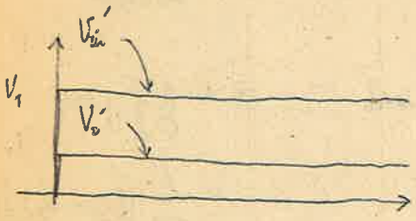
$R_2' = (R_2 // R_{in})$

$C_2' = (C_2 + C_{in})$



$v_{in} = V_1 u(t) - V_1 u(t - T/2) + V_1 u(t - T) - \cdots$

Since v_{in} is linear combination of step functions, if attenuator doesn't distorty "step" function, it doesn't distort v_{in}.

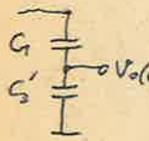


$v_o(0) = v_o(\infty)$

Find $v_o(0)$: Assume $v_{C_1}(0) = 0$, $v_{C_2'}(0) = 0$

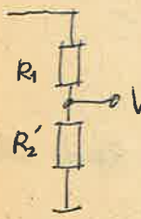
$v_{in}'(0) = V_1$

At t=0, C's are almost short cct. ∴ The current will pass through the capacitors.



$V_o(0) = \frac{C_1}{C_1 + C_2} V_1$

At $t = \infty$ the cct. is at steady state



$V_o(\infty) = \frac{R_2' V_1}{R_1 + R_2'}$

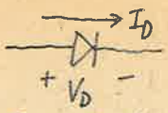
$v_o(0) = v_o(\infty)$

$C_1 R_1 + C_1 R_2' = R_2' C_1 + R_2' C_2'$

$\boxed{R_1 C_1 = R_2' C_2'}$

Nonlinear Waveshaping

Diode



$I_D = I_{rs}(e^{V_D/\alpha V_T} - 1)$

I_{rs} : reverse saturation current.

$V_T = \frac{kT}{q}$

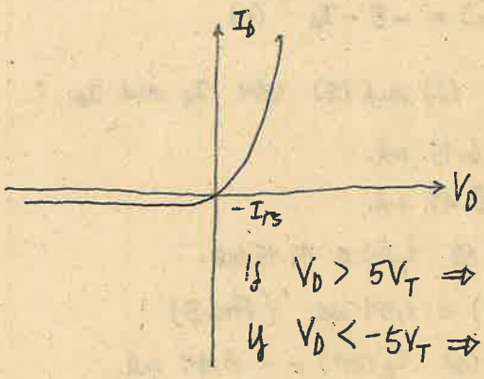
k : Boltzmann's constant

T : temperature in °K

q : electron charge.

$\alpha \approx 1$

$T = 300°K \Rightarrow V_T \approx 26\,mV.$

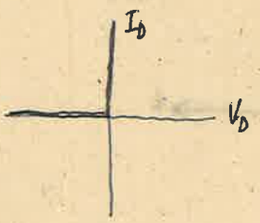


If $V_D > 5V_T \Rightarrow I_D = I_{rs} e^{V_D/V_T}$

If $V_D < -5V_T \Rightarrow I_D = -I_{rs}$.

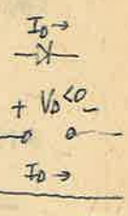
Diode models :

(1) Ideal diode :

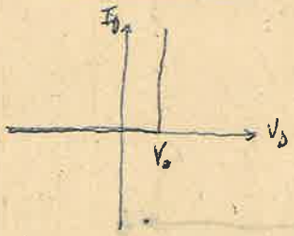


$V_D < 0 \Rightarrow I_D = 0$

$I_D > 0 \Rightarrow V_D = 0$

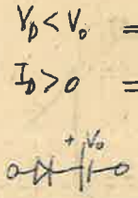


(2) First order model :

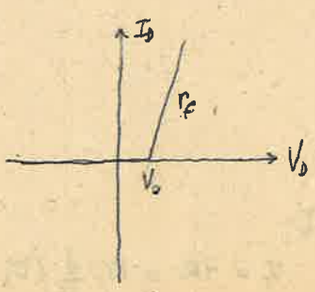


$V_D < V_o \Rightarrow I_D = 0$

$I_D > 0 \Rightarrow V_D = V_o$

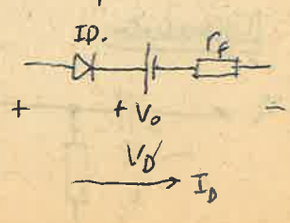


(3) Second order models

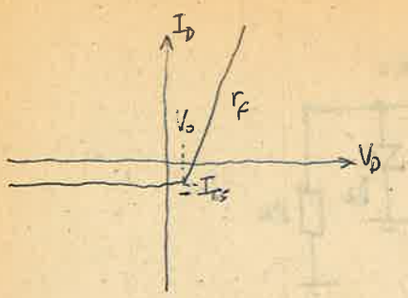


$V_D < V_o \quad I_D = 0$

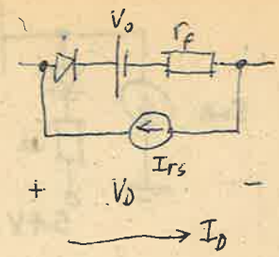
$I_D > 0 \quad r_f$



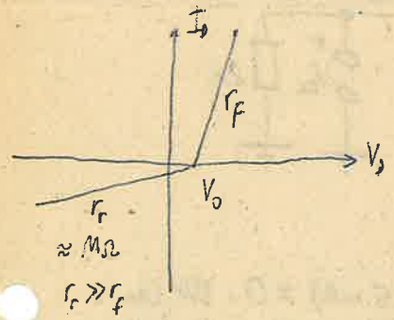
(4) Third order model. ①

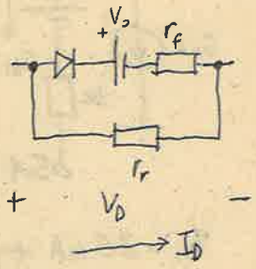


$V_D < V_o$ $\quad I_D = -I_{rs}$



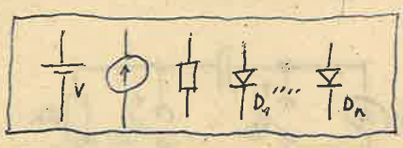
②





Finding the states of diodes in a network

Our network :



(1) Assume states for each diode.

● Replace ON diodes with a short cct.

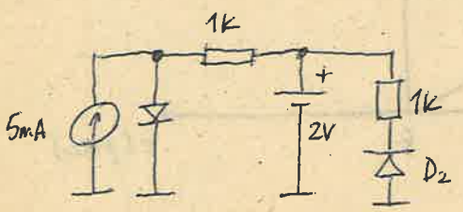
" OFF " " " open cct.

(2) Find the current through ON diodes, and voltages accross OFF diodes.

(3) If all currents thru ON diodes are positive and all voltages across OFF diodes are negative then the assumed stages are correct.

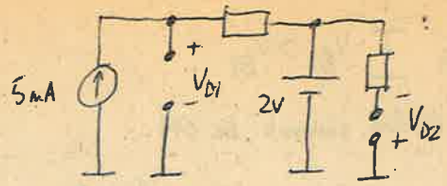
(4) If any contradiction, assume new states for the diodes and GO TO 2.

Example :



Find the states of the diodes, use first order method. ($V_o = 0.6$ V)

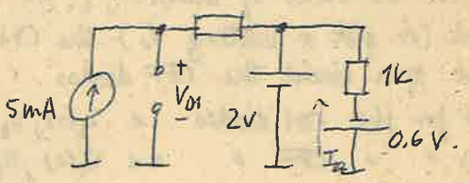
Assume D_1 OFF, D_2 OFF :



$V_{D2} = -2$ V. < 0.6 V ✓

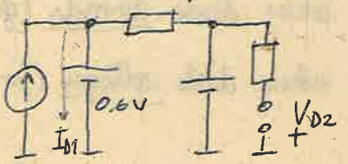
$V_{D1} = 7$V > 0.6 V ✗

Assume D_1 OFF, D2 ON :



$I_{D2} = -2.6$ mA < 0 ✗

Assume D_1 ON, D_2 OFF :

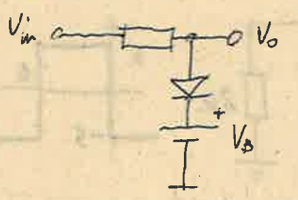


$V_{D2} = -2$V < 0.6 V ✓

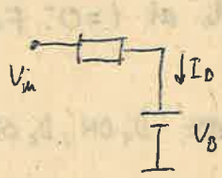
$I_{D1} = 6.4$mA > 0 ✓

D_1 ON
D_2 OFF

Example :

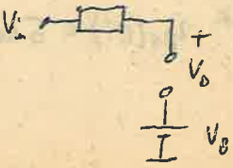


D ideal, Find V_{in} which makes D ON and OFF

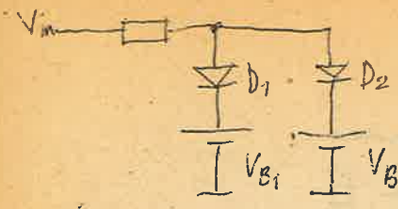


If $V_{in} > V_B$, $I_D > 0 \Rightarrow$ D ON

$V_o = V_B$



If $V_{in} < V_B$, $V_D < 0 \Rightarrow$ D OFF



EXERCISE

D ideal. Both diodes cannot be ON.

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* Piecewise linear solution of Networks Containing diodes and single energy storage element :

Algorithm

(1) At $t=0$ find the states of diodes - $\rightarrow t=0^-$ / $\searrow t=0^+$

(2) Short circuit (or put a battery V_0) the ON diodes and open circuit the OFF diodes.

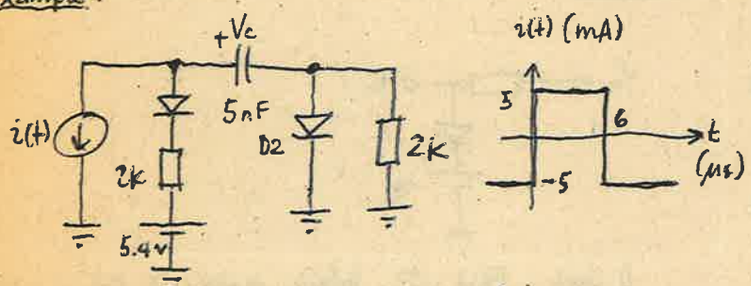
(3) Find $i_D(t)$ for the ON diodes i.e $i_D(0)$, $i_D(\infty)$
" $V_D(t)$ " " OFF " i.e $V_D(0)$, $V_D(\infty)$
Find τ
" $V_c(t)$ ($i_L(t)$)
" the waveform you interested.

(4) Find the times where diode currents (for ON ones) become zero.
Find the times where diode voltages (for OFF ones) become zero

(5) Change the state of the diode corresponding to the smallest time found in step (4). Replace the new model for this diode. Find the states of other diodes.
GO TO Step (2)

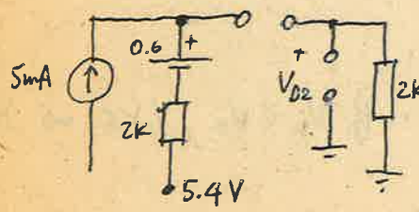
(6) Repeat until there is no change in diode states.

Example :



Use first order model for diodes. (With $V_\gamma = 0.6$ V)
The circuit is at steady-state at $t=0^-$. Find $V_A(t)$ for $t \geq 0$

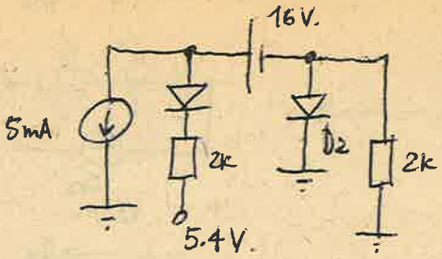
At $t=0^-$ C is open. Assume D_1 ON, D_2 OFF



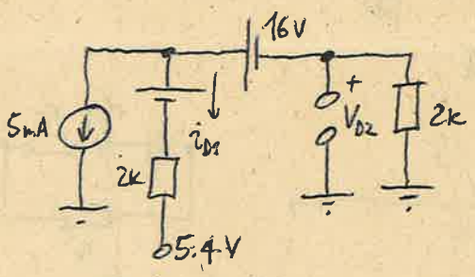
$V_{D2}(0^-) = 0 < 0.6$ V ✓
$i_{D1}(0^-) = 5$ mA ✓

$V_c(0) = 16$ V $= V_A(0^-)$

At $t=0^+$:

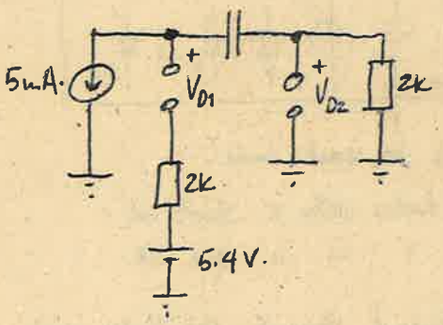


Assume D_2 OFF, D_1 ON



$i_{D1} = 2.5$ mA $+ (-2.5$ mA$) = 0$. We can't decide. 5 mA current source will discharge C. Hence $V_{D1}(0^+ + \varepsilon) < 0.6$ V

Let's look future situation! ∴ D_1 will be OFF



$$V_c(t) = 16 - \frac{1}{C}\int 5\times10^{-3}\,dt$$
$$= 16 - \frac{5\times10^{-3}}{5\times10^{-9}}t$$
$$= 16 - 10^6 t$$

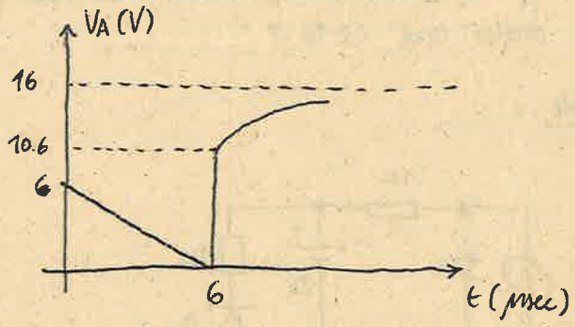
$V_A(t) = V_c(t) - 10 = 6 - 10^6 t$

$V_{D2}(t) = -10\text{V} < 0.6\text{V} \Rightarrow D_2$ always OFF

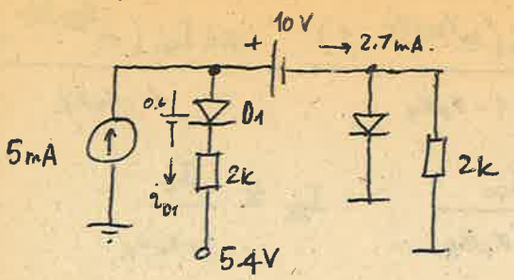
$V_{D1}(t) < 0.6$ V $\quad D_1$ always OFF

$V_c(6\mu\text{sec}) = 10$ V.

$V_A(6\mu\text{sec}) = 0$ V



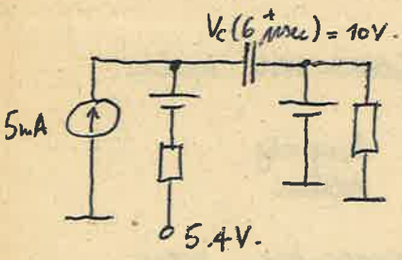
$t = 6\,\mu sec$



Assume D_1 ON, D_2 ~~OFF~~ ON

$i_{D1}(6\mu s^+) = 2.3\,mA > 0$ ✓

$i_{D2}(6\mu sec^+) = 2.4\,mA > 0$ ✓



$V_A(6^+) = 10.6\,V.$

$i_{D1}(\infty) = 5\,mA. \Rightarrow D_1$ is always ON.

$i_{D2}(\infty) = -0.3\,mA < 0$

$V_A(\infty) = 16\,V.$

$\tau = 10\,\mu sec.$

$$i_{D2}(t_1) = -0.3 + 2.7\,e^{-(t_1-6)/10} = 0$$

$$t_1 = 6 + 10 \ln \frac{2.7}{0.3} = 28\,\mu sec.$$

At $t = 28\,\mu sec$ D_2 will be OFF.

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For $6 < t < 28\,\mu sec.$

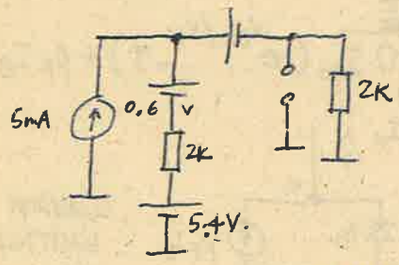
$$V_A(t) = 16 + [10.6 - 16]\,e^{-(t-6)/10}$$

$V_A(28) = 15.406\,V.$

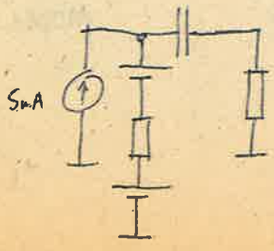
At $t = 28\,\mu sec.$ D_2 is OFF.

$V_c(28\,\mu sec) = V_A(28) - 0.6 = 14.806\,V.$

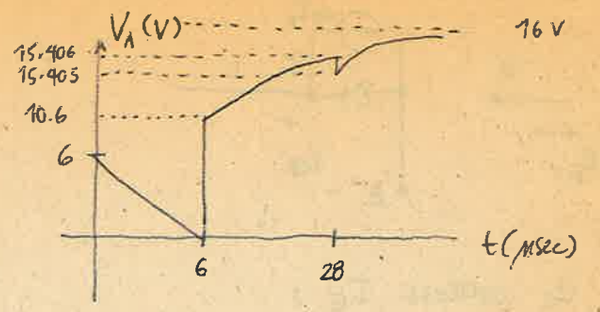
For $t = 28^+ \mu sec.$:



$$i_{D1}(28^+ \mu sec) = 2.5 + \frac{14.806 - 6}{4} = 4.7015\,mA > 0$$ ✓



$$V_A(28^+) = 5 + \frac{14.806 - 6}{4} \cdot 2 + 6 = 15.403\,V.$$



$V_{D2}(\infty) = 0 < 0.6\,V \Rightarrow D_2$ always OFF.

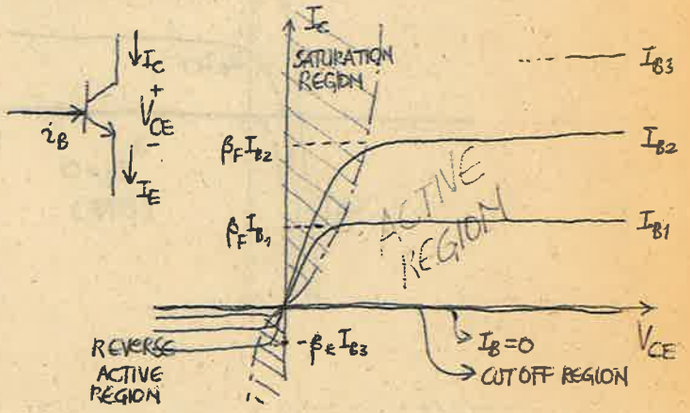
$i_{D1}(\infty) = 5\,mA > 0 \Rightarrow D_1$ " ON

$V_A(\infty) = 16\,V.$

$\tau = (5\,nF)(4K) = 20\,\mu sec.$

BIPOLAR JUNCTION TRANSISTOR

Common Emitter Configuration :



(1) Cutoff (OFF) region : $I_B = 0$

(2) Saturation (SAT) region : $-300\,mV < V_{CE} < 300\,mV.$ V_{CE} small. " for small power transistor "

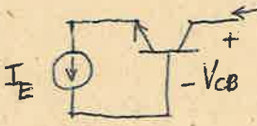
(3) Active region (ACT) :

$I_C = \beta_F I_B \quad V_{CE} > 0$

(4) Reverse active (REVACT) region :

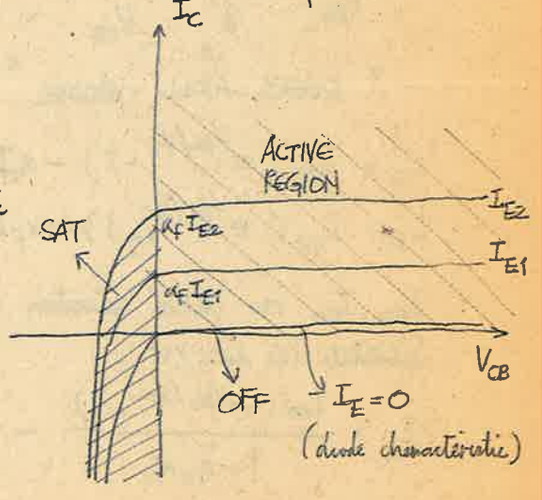
$I_C = -\beta_R I_B \quad V_{CE} < 0$

Common base configuration :

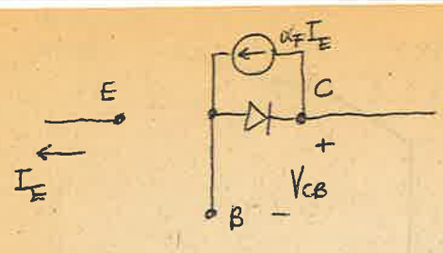


$\alpha_F \cong 1$

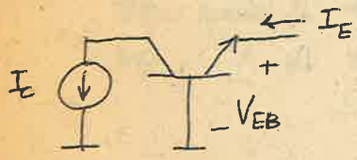
For $I_E = 0$ between C-B, there is reverse diode characteristic



I_E CONTROLS I_C

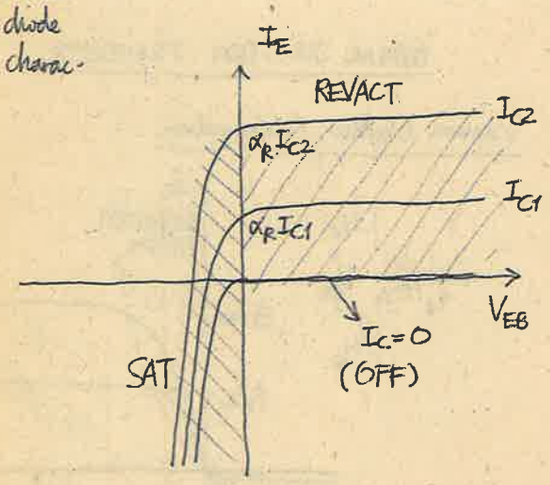


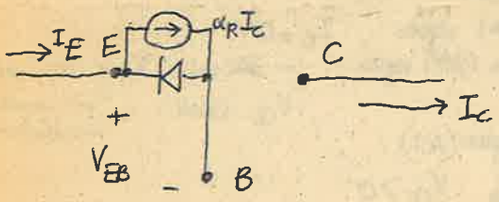
I_C CONTROLS I_E :



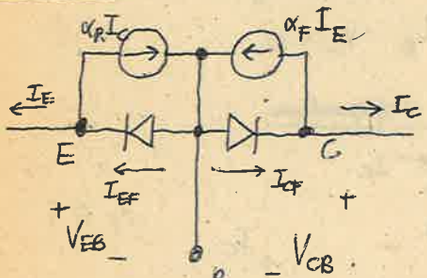
$I_C = 0$: reverse diode charac.

$\alpha_R < 1$





Combined model:



" EBERS-MOLL MODEL " (NPN)

$$I_E = I_{EO}\left(e^{V_{BE}/V_T} - 1\right) - \alpha_R I_C \quad (1)$$

$$I_C = I_{CO}\left(e^{V_{BC}/V_T} - 1\right) - \alpha_F I_E \quad (2)$$

I_{EO}, I_{CO} are reverse saturation currents of diodes

Substitute (2) into (1) :

$$I_E = \frac{I_{EO}\left(e^{V_{BE}/V_T} - 1\right)}{1-\alpha_F\alpha_R} - \frac{\alpha_R I_{CO}\left(e^{V_{BC}/V_T} - 1\right)}{1-\alpha_F\alpha_R}$$

Substitute (1) into (2) :

$$I_C = \frac{I_{CO}\left(e^{V_{BC}/V_T} - 1\right)}{1-\alpha_F\alpha_R} - \frac{\alpha_F I_{EO}\left(e^{V_{BE}/V_T} - 1\right)}{1-\alpha_F\alpha_R}$$

$$I_{CS} \triangleq \frac{I_{CO}}{1-\alpha_F\alpha_R} \qquad I_{ES} \triangleq \frac{I_{EO}}{1-\alpha_F\alpha_R}$$

$$I_E = I_{ES}\left(e^{V_{BE}/V_T} - 1\right) - \alpha_R I_{CS}\left(e^{V_{BC}/V_T} - 1\right) \quad (3)$$

$$I_C = I_{CS}\left(e^{V_{BC}/V_T} - 1\right) - \alpha_F I_{ES}\left(e^{V_{BE}/V_T} - 1\right) \quad (4)$$

(3) and (4) are EBERS-MOLL equations

$\alpha_F I_{ES} = \alpha_R I_{CS}$ Reciprocity relation

Common Emitter EBERS-MOLL MODEL

$$I_E = I_{EF} - \alpha_R I_C$$

Node equation at base : $I_C = -I_E - I_B$

$$I_E = I_{EF} + \alpha_R I_E + \alpha_R I_B$$

$$I_E = \frac{I_{EF}}{1-\alpha_R} + \frac{\alpha_R}{1-\alpha_R} I_B \qquad \beta_R \triangleq \frac{\alpha_R}{1-\alpha_R}$$

$$I_E = (\beta_R + 1) I_{EF} + \beta_R I_B$$

$$I_E = \underbrace{(\beta_R+1) I_{EO}}_{I_{ECO}}\left(e^{V_{BE}/V_T} - 1\right) + \beta_R I_B$$

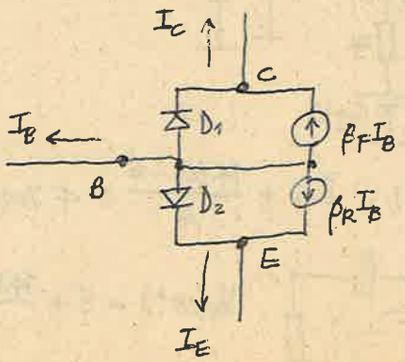
$$I_C = I_{CF} - \alpha_F I_E$$

$$I_E = -I_B - I_C$$

$$I_C = \frac{I_{CF}}{1-\alpha_F} + \frac{\alpha_F}{1-\alpha_F} I_B$$

$$\beta_F \triangleq \frac{\alpha_F}{1-\alpha_F}$$

$$I_C = \underbrace{(\beta_F+1) I_{CO}}_{I_{CEO}}\left(e^{V_{BC}/V_T} - 1\right) + \beta_F I_B$$



COMMON EMITTER NPN EBERS-MOLL MODEL

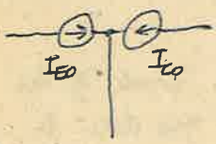
D_1 (CB)	D_2 (BE)	MODE OF OPERATION
OFF	OFF	CUTOFF
OFF	ON	ACTIVE
ON	OFF	REVERSE ACTIVE
ON	ON	SATURATION

Circuit Models can be found by using this chart.

Circuit Models for each Mode :

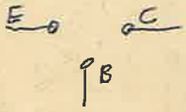
(1) CUTOFF $V_{CB} \ll -V_T$ $V_{CB} < V_o$

$V_{EB} \ll -V_T$ $V_{EB} < V_o$



Common-base NPN off transistor

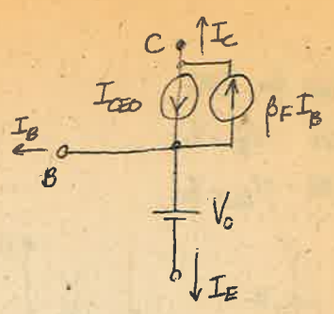
Simpler approximation:

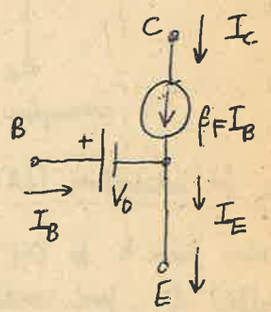


(2) ACTIVE

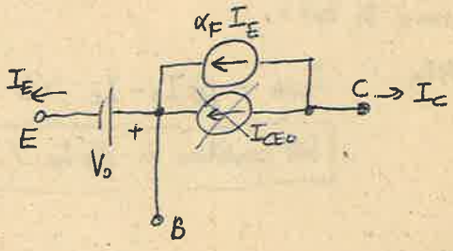
$V_{BE} = V_o$

$V_{BC} < V_o$

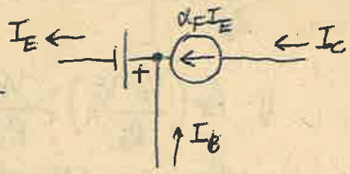




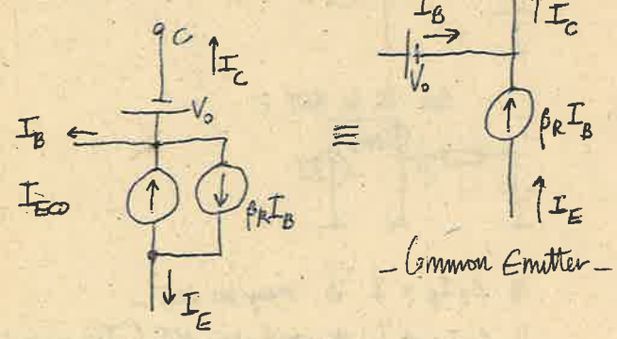
Common Emitter NPN Active Model



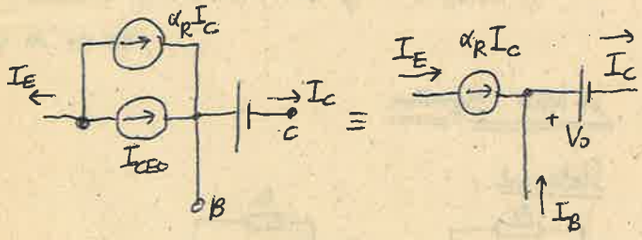
Common base NPN Active Model.



(3) REVERSE ACTIVE



– Common Emitter –



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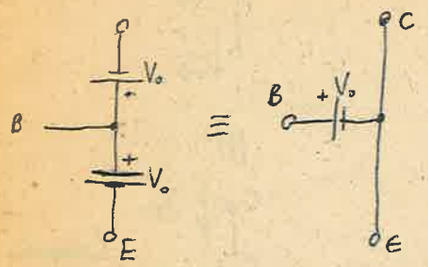
(4) Model for SAT

D_1 ON $V_{BE} = V_0$

D_2 ON $V_{BE} = V_0$

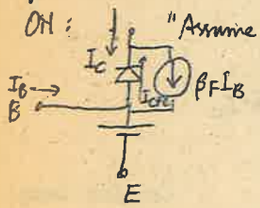


assumption: $V_{CE,SAT} = 0$

Conditions for saturation (SAT)

Both diodes have to be ON.

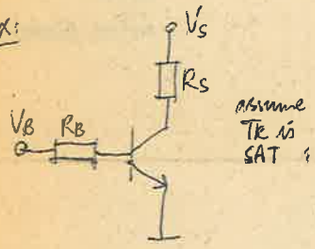
Given D_2(BE) ON, find conditions which make D_1 ON: "Assume D_1 ON"



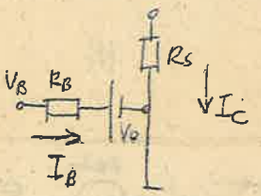
$I_{CFE} = \beta_F I_B - I_C > 0$

SAT condition is $\beta_F I_B > I_C$

ex:



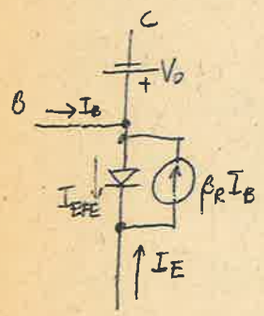
assume TR is SAT:



If $\beta_F \left(\frac{V_B - V_0}{R_B}\right) > \frac{V_S}{R_S}$

then Tr. is SAT really.

(II) Given D_1(BC) ON, find the conditions which make D_2(BE) ON:



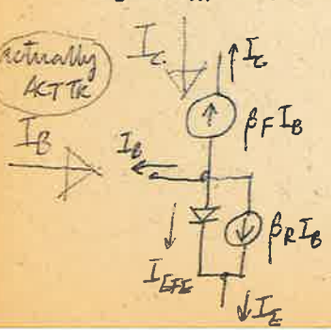
$I_{EFE} = \beta_R I_B - I_E > 0$

$\beta_R I_B > I_E$

Conditions for ACT

D_1(BC) is OFF → 1) $V_{BC} < V_0$
2) $V_{BE} = V_0$

D_2(BE) is ON



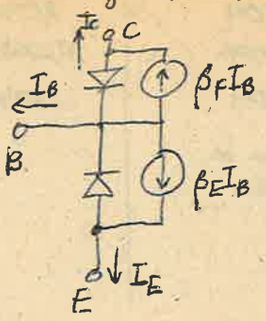
$I_{EFE} = -(\beta_F + \beta_R + 1) I_B > 0$

($\beta_F + \beta_R + 1 > 0$)

$I_B < 0$ it says actual direction of I_B is inwards of ACT transis.

PNP BJT

Change the directions of the diodes:



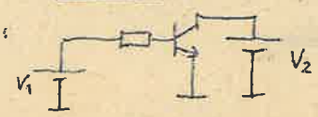
Common Emitter Ebers-Moll Model for PNP-BJT

160382

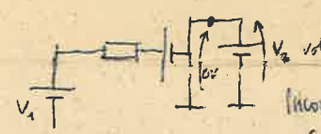
Finding the states of a transistor in a network

1) Assume a state for TR.
2) Replace the equivalent model, check if the conditions which bring TR to this state is satisfied.
3) There has to be no circuit inconsistency.

eg:

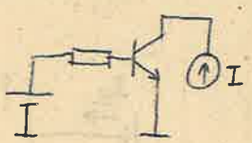


is TR in SAT mode?

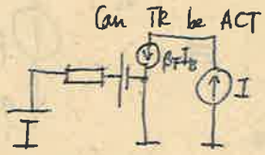


TR cannot be SAT. (Two voltage sources are (0V, V_2 volts) in parallel)

eg:



Can TR be ACT?

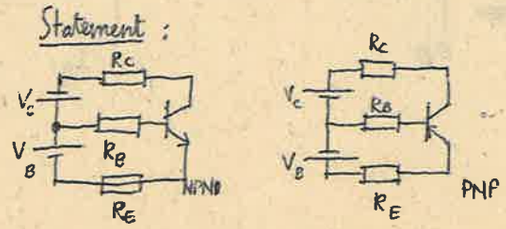


If $\beta_F I_B = I$ it may be ACT.

If $\beta_F I_B \neq I$ it can't be ACT (Two current sources are in series)

A better algorithm:

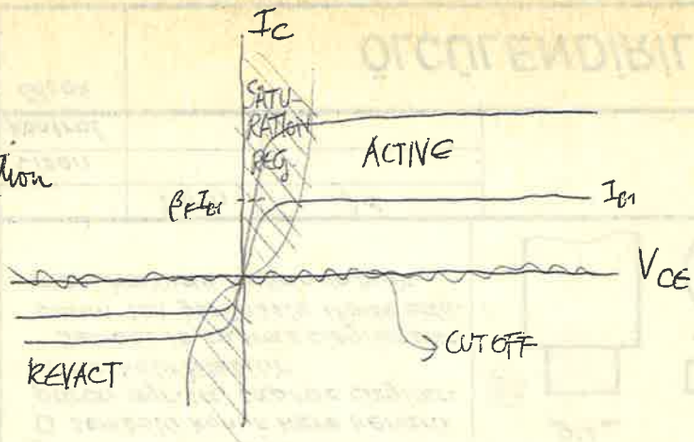
Statement:

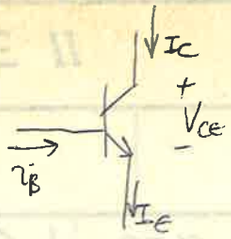


In these networks if $V_B > V_C$ TR's cannot be REVACT.

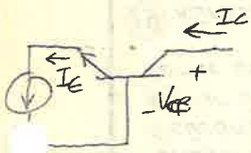
BIPOLAR JUNCTION TRANSISTOR : [NPN]

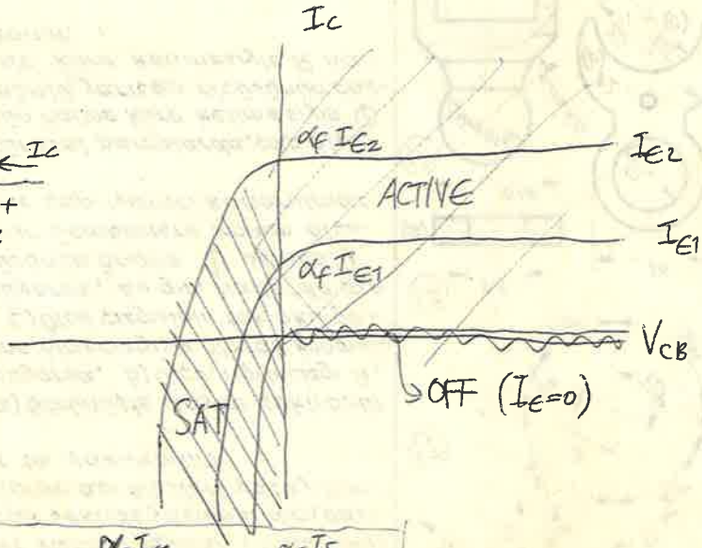
Common Emitter Configuration



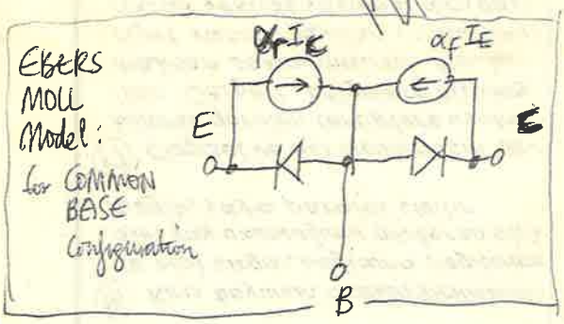


Common Base Configuration





EBERS MOLL Model: for COMMON BASE Configuration



Algorithm :

NPN

Remove TR if $V_{BE} < V_0$ TR is OFF

$V_{BC} < V_0$

$V_{BE} > V_{BC}$

~~ALGORITHM FOR 2 TRANSISTORS~~

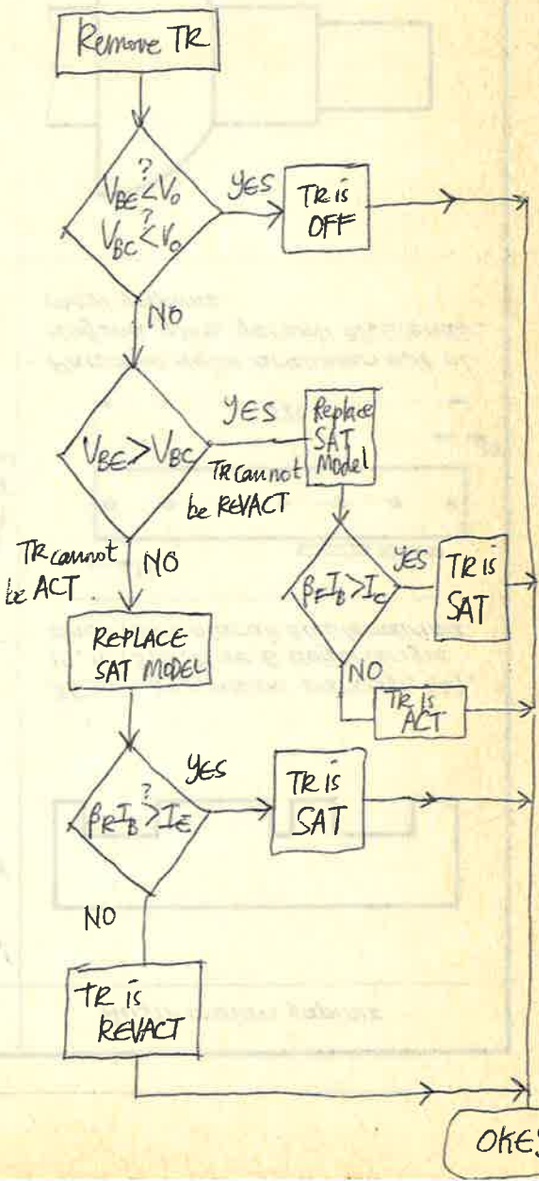
~~(1) Remove T_1~~
(2) Find the state of T_2 when T_1 removed.
(3) ~~Find~~ Put model for T_2
(4) Find the state of T_2
(5) Put new model for T_1
(6) Find the state of T_2
(7) Put model for T_2
(8) Find the state of T_1

Algorithm For 2 Transistors

(1) Decide which model to be replaced for T2 when T1 removed (ie SAT / OFF)
(2) Find the state of T1

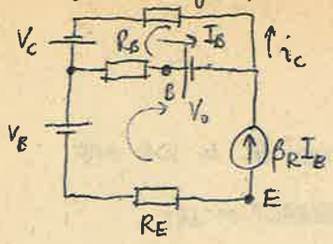
~~Algorithm~~

Flowchart for NPN TR



Proof: (by contradiction) :

Assume TR is REVACT and then observe that the conditions for REVACT TR are not satisfied.



$$V_B = R_B I_B + V_{BE} + \beta_R I_B R_E$$

$$V_C = R_B I_B + V_o + R_C(\beta_R + 1) I_B$$

$$V_B - V_C = V_{BE} - V_o - I_B[\beta_R R_E + (\beta_R + 1) R_C]$$

Conditions for REVACT:

$V_{BE} < V_o$, $I_B > 0$

$$V_{BE} - V_o = \underbrace{(V_B - V_C)}_{>0} + I_B[\beta_R R_E + (\beta_R + 1) R_C]$$

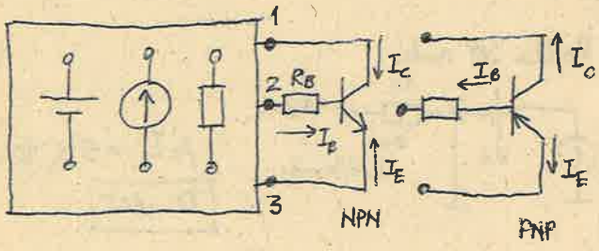
If $V_{BE} < V_o$ then $I_B < 0$ ✗
If $I_B > 0$ then $V_{BE} > V_o$ ✗
} TR cannot be REVACT.

□

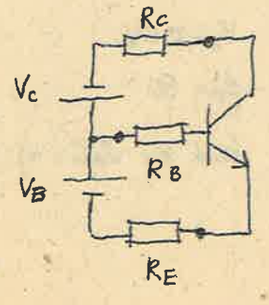
Statement: If in above networks $V_B < V_C$ then TR's cannot be ACT.

Proof: Homework.

Algorithm :



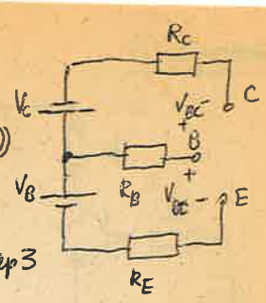
Find Thevenin eq. circuits between 1-2 and 2-3.



→ PNP

1) Remove TR and then find V_{BE} (V_{EB}), V_{BC} (V_{CB})
if V_{BE} (V_{EB}) $< V_o$ and V_{BC} (V_{CB}) $< V_o$
the TR is OFF.

Otherwise Go to step 2.



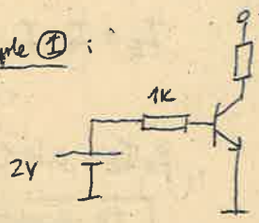
2) a) If V_{BE} (V_{EB}) $> V_{BC}$ (V_{CB})
TR can't be REVACT, TR is either • ACT or SAT Go to step 3

b) If V_{BE} (V_{EB}) $< V_{BC}$ (V_{CB})
TR can't be ACT. TR is either REVACT or SAT
Go to step 4.

3) Replace TR by SAT model.
If $\beta_F I_B > I_C$ TR is SAT.
If not it is ACT.

4) Replace TR by SAT model
If $\beta_R I_B > I_E$ TR is SAT
If not TR is REVACT.

example ① :



$\beta_F = 10$
$V_B = 0.6$ V.

Remove TR, $V_{BE} = 2V > 0.6$ V ⇒ TR isn't OFF
$V_{BC} = -18$ V.

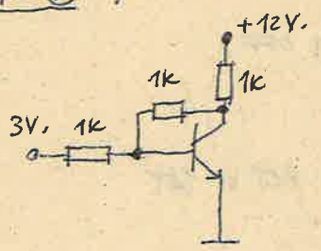
$V_{BE} > V_{BC}$
⇒ TR is ACT or SAT

$I_B = 1.4$ mA.

$I_C = 20$ mA.

$\beta_F I_B = 14 < 20$ **TR ACT**

example ② :



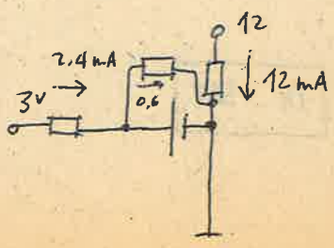
$V_o = 0.6$ V.
$\beta_F = 50$ V.

Remove TR :

$V_{BE} = 6$ V. > 0.6 ⇒ TR not OFF.

$V_{BC} = -3$ V

$V_{BE} > V_{BC}$ ⇒ TR is SAT or ACT



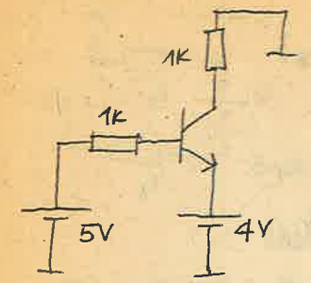
$I_B = 2.4 - 0.6 = 1.8$ mA.

$I_C = 12.6$ mA.

$\beta_F I_B = 80 > 12.6$

TR SAT

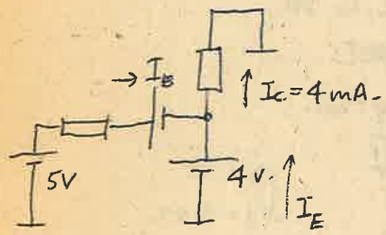
example ③ :



$\beta_R = 1$
$V_o = 0.6$

Remove TR:
$V_{BE} = 1\ V.$
$V_{BC} = 5\ V$
} TR is not OFF

$V_{BC} > V_{BE} \Rightarrow$ TR REVACT or SAT :



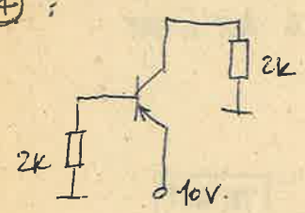
$I_B = \frac{5-4.6}{1K} = .4\ mA.$

$I_E = I_C - I_B = 4 - 0.4$
$= 3.6$

$\beta_R I_B = 0.4 < 3.6$

TR REVACT

example ④ :

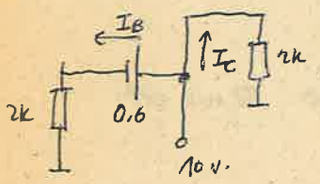


$\beta_F = 100$
$V_o = 0.6\ V.$

Remove TR:
$V_{EB} = 10\ V.$
$V_{CB} = 0$
} TR is not OFF.

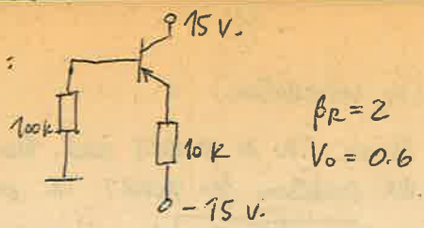
$V_{EB} > V_{CB} \Rightarrow$ TR is ACT or SAT

SAT model;



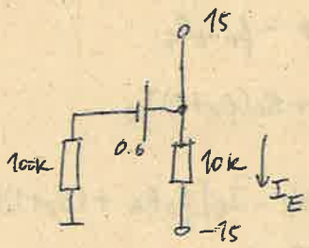
$I_B = 4.7\ mA$
$I_C = 5\ mA.$
$\beta_F I_B = 470 > 5$ TR. SAT

example ⑤ :



$\beta_R = 2$
$V_o = 0.6$

Remove TR:
$V_{EB} = -15\ V.$
$V_{CB} = 15\ V > 0.6 \Rightarrow$ TR is not OFF.
$V_{CB} > V_{EB}$ TR is REVACT or SAT

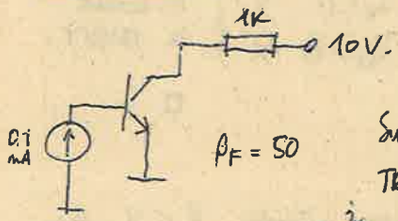


$I_B = \frac{15-0.6}{100} = 0.144\ mA.$

$I_E = \frac{30}{10} = 3\ mA.$

$\beta_R I_B = 0.288 < I_E = 3\ mA.$ TR REVACT

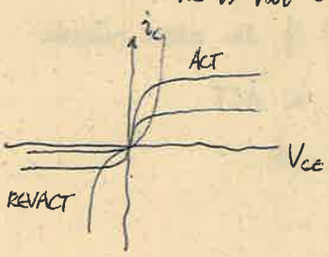
example ⑥ :



$\beta_F = 50$

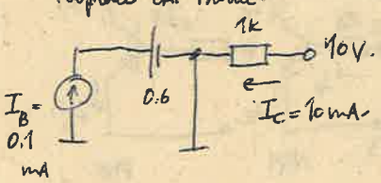
Since $I_B = 0.1\ mA$
TR is not OFF.

$V_{BE} > V_{BC}$
$V_B - V_E > V_B - V_C$
$V_E < V_C$
↑
ACT or SAT NPN.



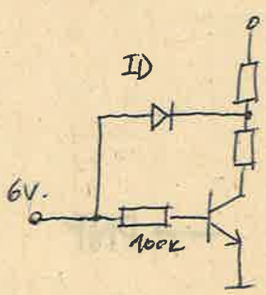
TR is not REVACT

Replace SAT model:



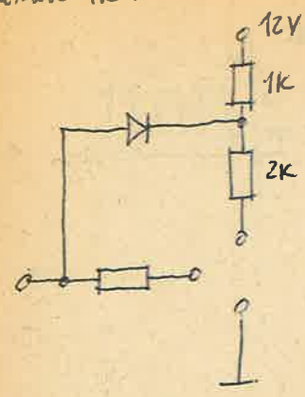
$\beta_F I_B = 5 < 10\ mA.$
TR ACT

example ⑦ :



$V_o = 0.6\ V.$
$\beta_F = 50$
find the states of D and TR.

Remove TR:



Find the state of Diode:

Assuming D is OFF;

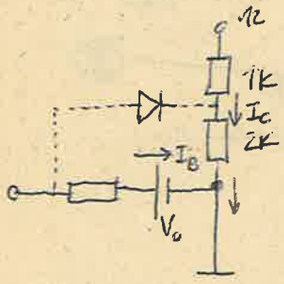
$V_D = 6 - 12 = -6$ ✓ D is OFF.

$V_{BE} = 6$ V.

$V_{BC} = -6$ V. TR is not OFF.

$V_{BE} > V_{BC}$ TR is SAT or ACT

Replace SAT model:



Again Find the state of D:

Assume Diode is OFF:

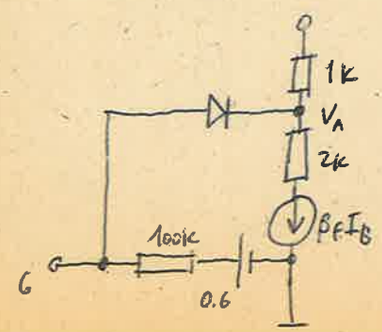
$6 - \frac{12}{3} \cdot 2 = -2$ V. < 0 ✓ D is OFF.

$I_B = \frac{6 - 0.6}{100K} = 0.054$ mA.

$I_C = \frac{12}{3K} = 4$ mA.

$\beta_F I_B = 2.7 < 4$ TR ACT

We must find again state of D because when we were finding the state of diode we have assumed that the TR is SAT.



$I_B = 0.054$ mA.

Assume D is OFF.

$\beta_F I_B = 2.7$ mA.

$V_A = 12 - (1K)(2.7\,mA)$

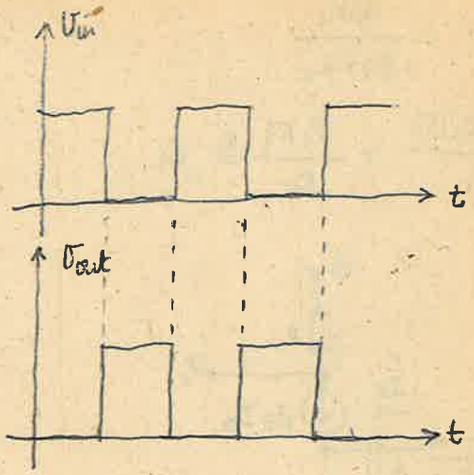
$= 9.3$ V.

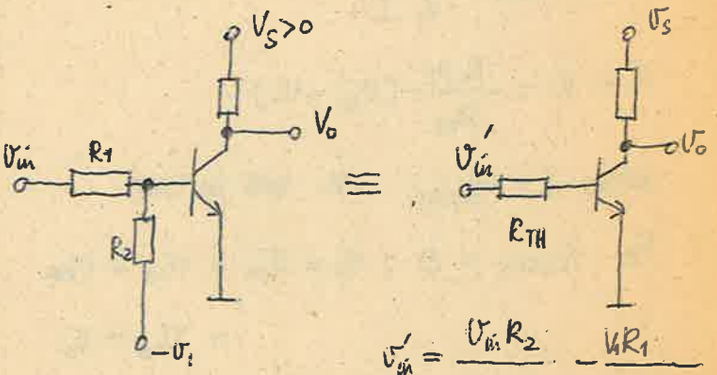
$V_D = 6 - 9.3 = -3.3\,V < 0$

D is OFF ✓

TRANSISTOR INVERTER

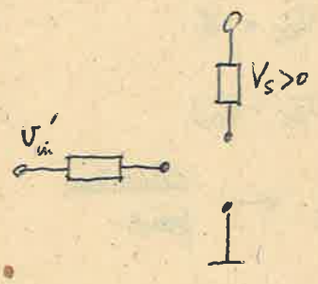
is used to invert a high level input to a low level output and a low input to high output.





$$V'_{in} = \frac{V_{in} R_2}{R_1 + R_2} - \frac{V_1 R_1}{R_1 + R_2}$$

$R_{TH} = R_1 // R_2$



$V_{BE} = V'_{in}$

$V_{BC} = V'_{in} - V_S$

$V_{BE} > V_{BC}$

∴ TR cannot be REVACT

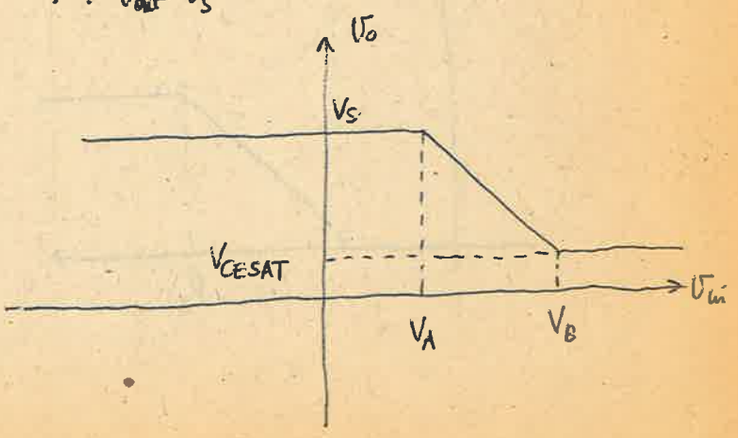
Let V_{in} be large negative:

Since $V_{BE} = V'_{in} < V_o$

$V_{BC} = V'_{in} - V_S < V_o$

∴ TR is OFF.

∴ $V_{out} = V_S$

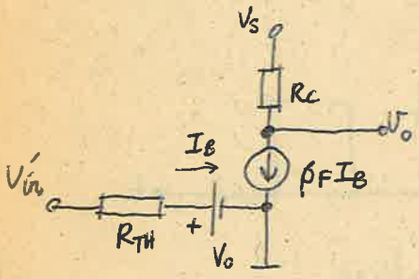


When $V_{in}' = V_{on}$ BE diode is ON
BC diode is OFF

∴ TR is ACT.

$$V_o = \frac{V_{in} R_2}{R_1+R_2} - \frac{V_1 R_1}{R_1+R_2}$$

$$V_{in}' = \frac{(R_1+R_2)V_o}{R_2} + \frac{V_1 R_1}{R_2} \triangleq V_A$$



$$V_o = V_S - \frac{R_C \beta_F}{R_{TH}} (V_{in}' - V_o)$$

when $V_o = V_{CESAT}$ TR will be SAT

For $V_{CESAT} = 0$, $V_o = V_{CE} = V_{CB} + V_{BE}$

$$= V_{CB} + V_o$$

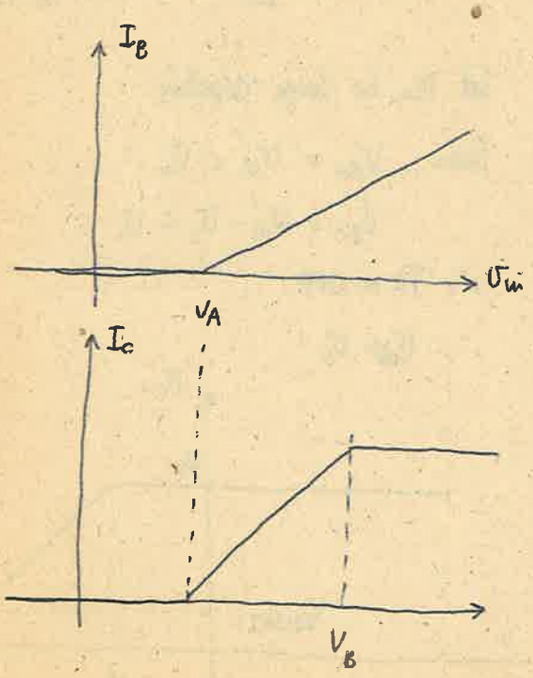
$$0 = V_{CB} + V_o$$

$$V_{CB} = -V_o$$

$$V_{BC} = V_o$$

$$0 = V_S - \frac{\beta_F R_C}{R_{TH}} (V_{in}' - V_o)$$

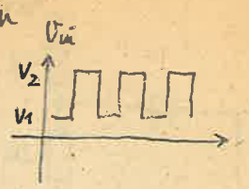
$$V_{in}' = \frac{R_{TH} V_S}{\beta_F R_C} + V_o \leftarrow \text{saturation point.}$$

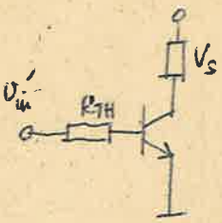


How to choose R_1, R_2 ?

Choose R_1, R_2 such that when

$V_{in} = V_2$ TR is SAT
$V_{in} = V_1$ TR is OFF



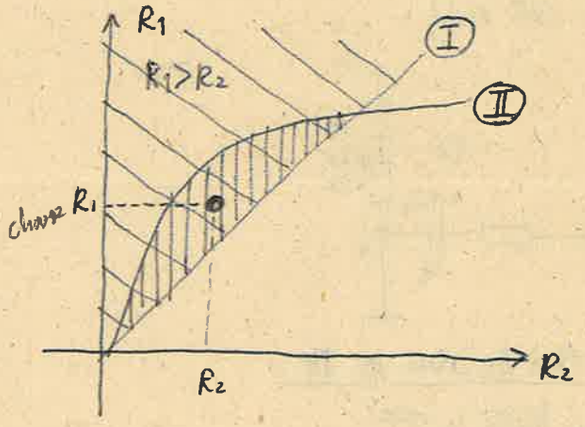


$$V_{in}' = \frac{V_{in} R_1}{R_1+R_2} - \frac{V_1 R_1}{R_1+R_2} < V_{BE_{OFF}} < 0$$

$$R_1 \gtrless (\quad) R_2 \quad (I)$$

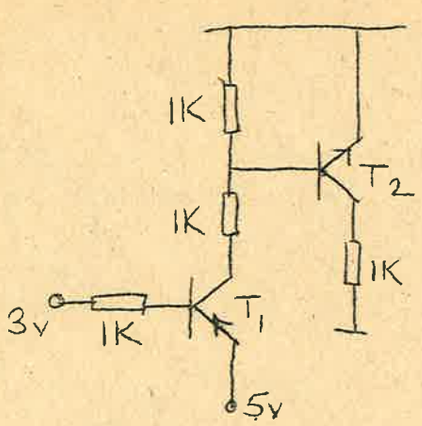
when $V_{in} = V_2$ $\beta_F I_B > I_C$

$$\beta_F * \left[\frac{V_{in}' - V_o}{R_{TH}}\right] > \frac{V_S}{R_C} \quad (II)$$



EE 411

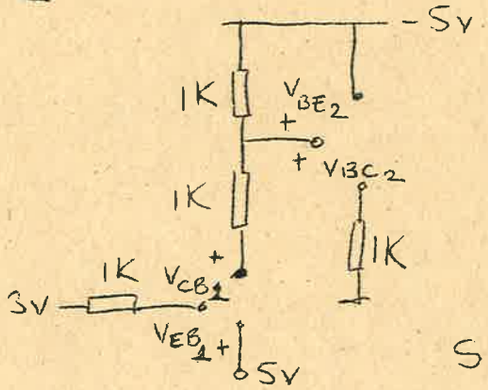
An Example on Finding The States of Transistors



$\beta_F = 100$

$V_0 = 0.6V$.

Remove T_1, find V_{EB_1} and V_{CB_1} and check if T_1 is OFF. To find V_{EB_1} and V_{CB_1}, we have to know the state of T_2 when T_1 is removed.



$V_{BE_2} = 0V < 0.6V$

$V_{BC_2} = -5V < 0.6V$

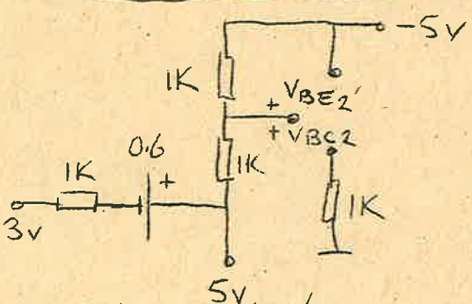
$\Rightarrow T_2$ is OFF.

$\therefore V_{EB_1} = 2V \Rightarrow T_1$ not OFF

$V_{CB_1} = -8V$

Since $V_{EB_1} > V_{CB_1} \Rightarrow T_1$ is ACT or SAT.

Now, put SAT. model for T_1 and check if $\beta_F I_{B_1} > I_{C_1}$. But to find I_{B_1} and I_{C_1}, we have to know the state of T_2 when T_1 is replaced by SAT model.

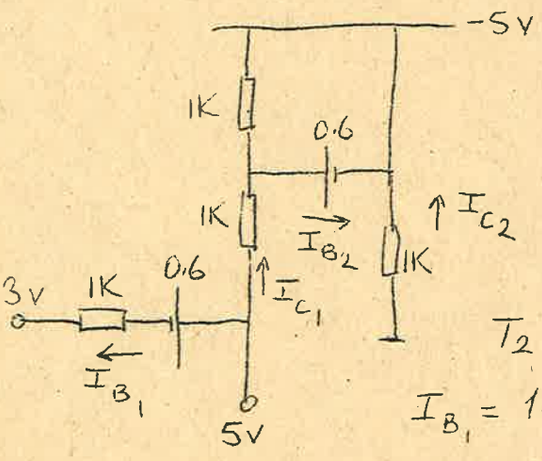


$V_{BE_2} = 5V > 0.6V \Rightarrow T_2$ is not OFF.

$V_{BC_2} = 0V$.

$V_{BE_2} > V_{BC_2} \Rightarrow T_2$ is ACT or SAT.

Replace T_2 with SAT model and find its state.



$I_{C_2} = 5mA$ $\quad I_{C_1} = \frac{10 - 0.6}{1K} = 9.4mA$

$I_{B_2} = I_{C_1} - 0.6mA = 8.8mA$.

$\beta_F I_{B_2} = 880mA > I_{C_2} = 5mA \Rightarrow T_2$ SAT.

$\therefore$ when T_1 is replaced by SAT model T_2 is SAT. Now check if $\beta_F I_{B_1} > I_{C_1}$

$I_{B_1} = 1.4mA$. $\therefore \beta_F I_{B_1} = 140mA > I_{C_1} = 9.4mA$.

$\therefore T_1$ is SAT.

Hence the states of transistors are T_1 SAT, T_2 SAT

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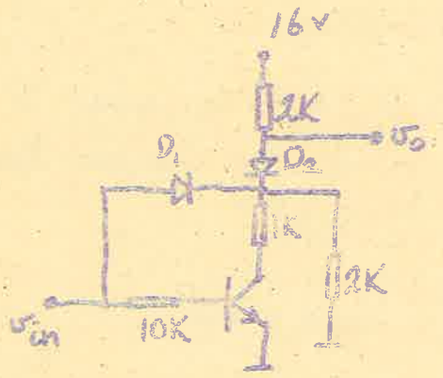
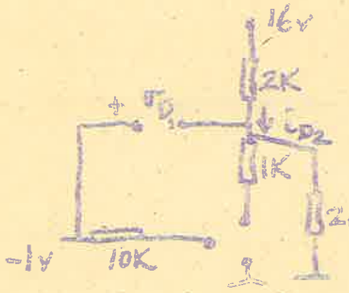
✓ Example on finding the states of transistors and diodes



D_1 and D_2 are ideal diodes. For the transistor we have $\beta_F = 20$ and $V_\gamma = 0.6$V. Find and plot v_o vs. v_{in} for $-1V \le v_{in} \le 20V$.

Solution: Begin with $v_{in} = -1$V. Remove transistor find the states of diodes, measure v_{BE} and v_{BC} and decide on the state of the transistor:

Remove TR and assume D_1 OFF, D_2 ON:

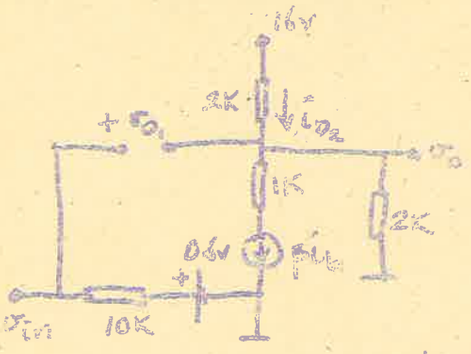


$v_{D_1} = -1 - 8 = -9V < 0$ ✓
$i_{D_2} = 4mA > 0$ ✓
$\Rightarrow D_1$ OFF, D_2 ON.

$v_{BE} = -1V < 0.6V$
$v_{BC} = -1 - 8 = -9V < 0.6V$
$\Rightarrow$ TR OFF.

$\therefore v_o = 8$V.

TR becomes ACT when $v_i = 0.6$V. When $v_i = 0.6$, i_b is still zero. $\therefore i_c$ is also zero. $\because v_o = 8$V, $\therefore D_2$ is still ON and D_1 is OFF. $\therefore$ we have:



TR becomes SAT when $\beta i_b = i_{c_{SAT}}$

$i_{c_{SAT}} = \frac{16}{4} = 4$mA.

$\beta i_b = \frac{20(v_{in} - 0.6)}{10K}$

$\beta i_b = i_{c_{SAT}} \Rightarrow v_{in} = 2.6$V.

When TR is SAT, $v_o = 4$V.

Check the states of the diodes when TR is SAT:

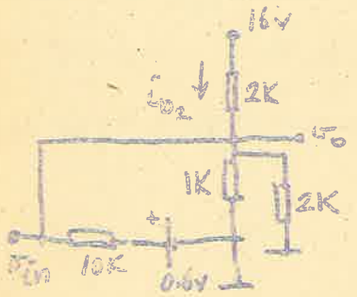
$v_{D_1} = v_{in} - v_o = 2.6 - 4 = -1.4V < 0 \Rightarrow D_1$ is OFF

$i_{D_2} > 0 \Rightarrow D_2$ is still ON.

As v_{in} increases i_b increases. $\therefore$ TR remains SAT. But when $v_{in} = v_0 = 4v$, D_1 becomes ON.

$\therefore$ for $2.6v < v_{in} < 4v$, TR is SAT, D_2 is ON, D_1 is OFF.

For $v_{in} = 4v$, since D_1 is ON we have $v_0 = v_{in}$



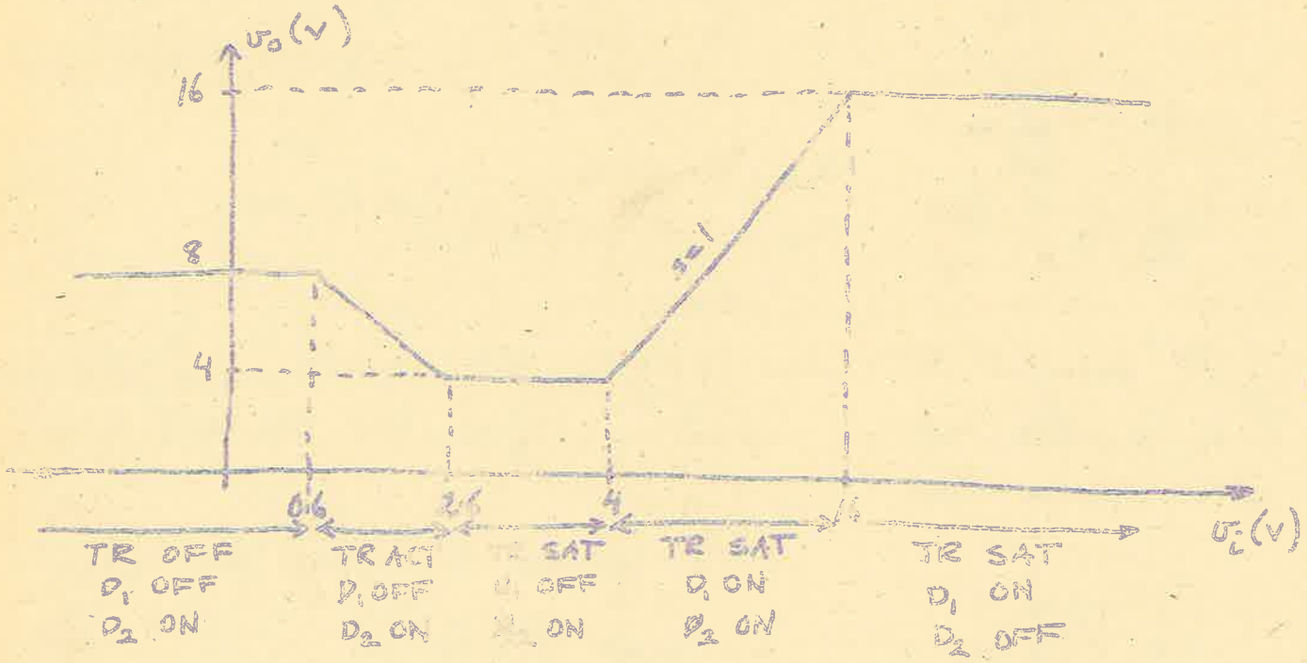
Find the states of TR and D_2 when D_1 is OFF: From the figure we observe that $v_{in} > 0$. $\therefore$ D_2 is still ON.

$$i_b = \frac{20(v_{in} - 0.6)}{10K} \qquad i_{bSAT} = \frac{v_{in}}{1K}$$

$2(v_{in} - 0.6) > v_{in}$ for $v_{in} > 4v$ $\therefore$ TR is SAT

$v_0 = v_{in}$.

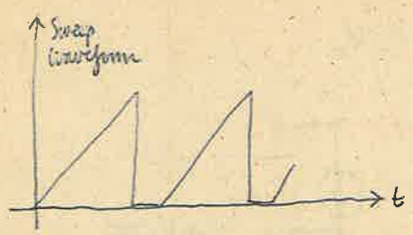
When $v_{in} = 16v$, D_2 becomes OFF and $v_0 = 16v$.



260382

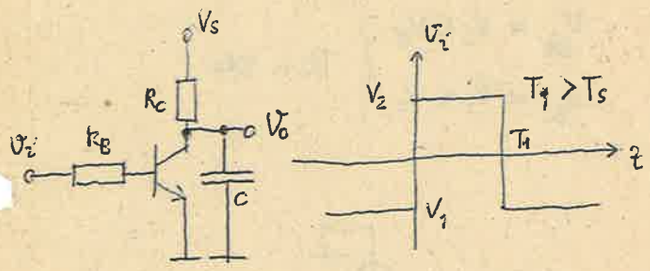
SWEEP CIRCUITS

generate periodic signals that change linearly (almost linearly) with time.



Voltage sweep generators

Sweep generator using an inverter:



Choose V_1 such that TR is OFF. ie $V_1 < V_o$

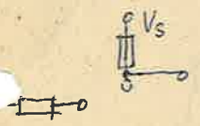
" V_2 " " " " SAT ie $\frac{\beta_F (V_2 - V_o)}{R_B} > \frac{V_S}{R_C}$

$V_2 > V_o$

At $t = 0^-$ the circuit is at steady-state.

$\therefore$ C is open circuit.

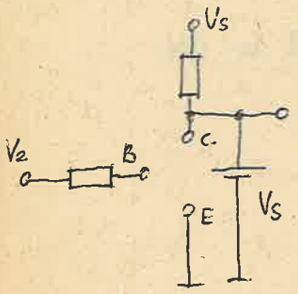
Since $v_i = V_1 < V_o$, TR is OFF.



$v_o(0^-) = V_S$

$v_o(0^-) = v_c(0^-) = V_c(0^+)$

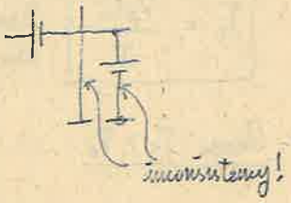
At $t = 0^+$



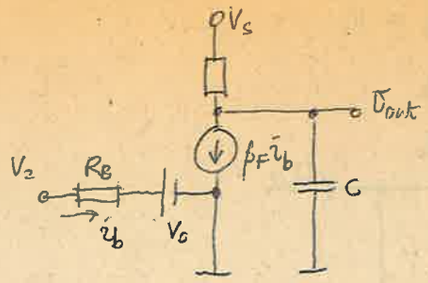
$v_{BE} = V_2 > V_o$ } TR ACTor SAT

$v_{BC} = V_2 - V_S$ }

(it cannot be SAT):



$\therefore$ TR is ACT.



$i_b = \frac{V_2 - V_o}{R_B}$

$i_c = \frac{\beta_F (V_2 - V_o)}{R_B}$ Constant.

all waveforms are exponential.

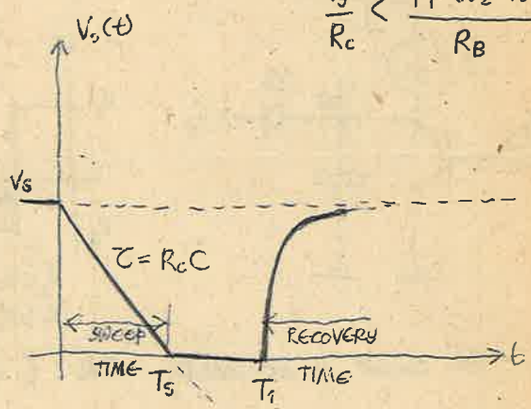
$V_{out}(0^+) = v_c(0) = V_S$

$v_{out}(\infty) = V_S - R_C \beta_F \frac{(V_2 - V_o)}{R_B}$

$\tau = R_C C$

$v_{out}(\infty) < 0$ because $\frac{V_S}{R_C} - \frac{\beta_F (V_2 - V_o)}{R_B} \overset{?}{<} 0$

$\frac{V_S}{R_C} \overset{\checkmark}{<} \frac{\beta_F (V_2 - V_o)}{R_B}$

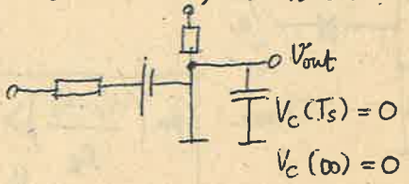


$$v_{out}(t) = V_S - \frac{\beta_F R_C (V_2 - V_o)}{R_B} + \left[\frac{R_C \beta_F (V_2 - V_o)}{R_B}\right] e^{-t/R_C}$$

$v_{out}(T_S) = 0$

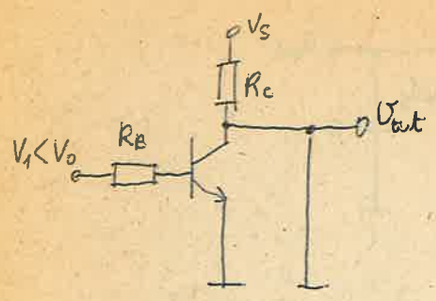
$$T_S = R_C C \ln \frac{\left[\frac{R_C \beta_F (V_2 - V_o)}{R_B}\right]}{\left[\frac{\beta_F R_C (V_2 - V_o)}{R_B} - V_S\right]}$$

For $T_S < t < T_1$, TR is SAT.:

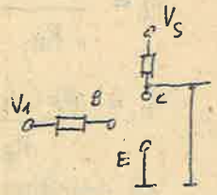


$V_c(t) = 0 \Rightarrow$ C is open TR is SAT.

for $t > T_1$: $v_i = V_1$

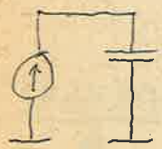


$v_{BE} = V_1 < V_0$
$v_{BC} = V_1 < V_0$
} Tr is OFF.

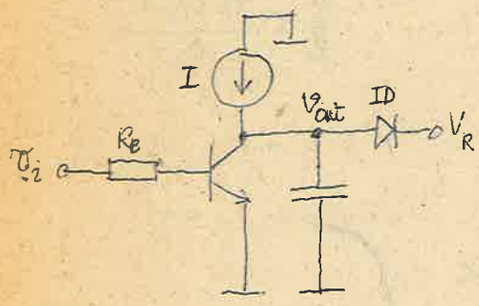


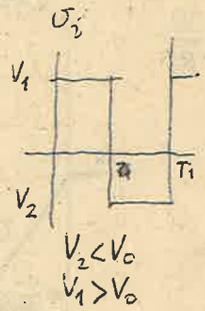
$v_{out}(\infty) = V_S$
$\tau = R_C C$

Current charging :

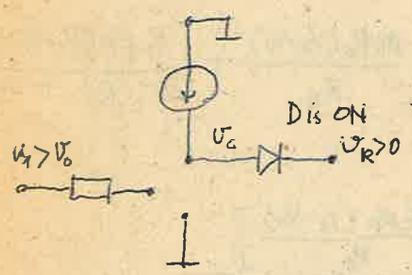


$V_C = V(0) + \frac{1}{C}\int I\,dt$

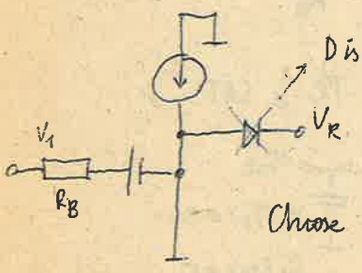




$t = 0^-$: the circuit is at steady-state. C is open.



$v_C = V_R$
$v_{BE} = V_1 > V_0$
$v_{BC} = V_1 - V_R$
$V_{BE} > V_{BC} \Rightarrow$ TR ACT or SAT

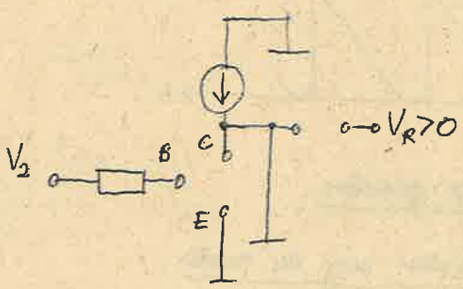


Choose $\boxed{\beta_F\left(\frac{V_1 - V_0}{R_B}\right) > I \Rightarrow \text{Tr is SAT}}$

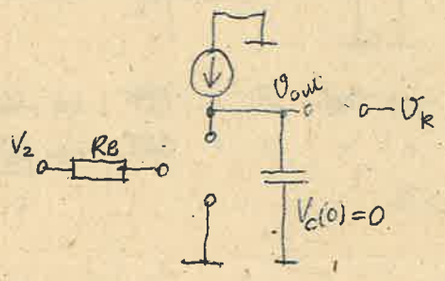
$\therefore v_{out}(0^-) = 0$
$v_C(0) = 0$

$\underline{t = 0^+}$:

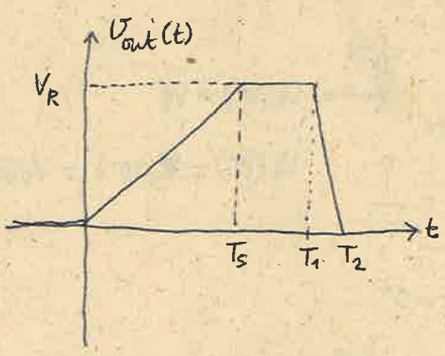
$v_i = v_2 < V_0$



$v_{BE} = V_2 < V_0$
$v_{BC} = V_2 < V_0$
} TR is OFF.



$v_o(t) = \frac{1}{C}\int_0^t I\,d\tau = \frac{I}{C}t$



When $v_{out}(t) = V_R$, D will be ON

$v_{out}(T_S) = \frac{I}{C} \cdot T_S = V_R$.

$\boxed{T_S = \frac{V_R C}{I}}$ Sweep time

Choose $T_1 > T_S$: For $T_S < t < T_1$:

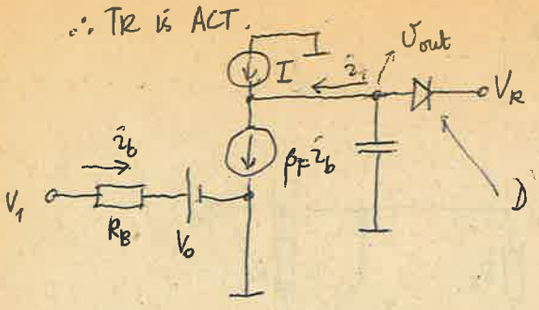
$v_{out}(t) = V_R \quad v_C(T_1) = V_R$

At $t = T_1^+$: $v_i = V_1 > V_0$

BE diode is ON $\Rightarrow$ Tr cannot be OFF.

TR cannot be SAT, otherwise inconsistency.

∴ TR is ACT.



$$\beta_F i_b = \beta_F \frac{(V_1 - V_o)}{R_B} > I$$

$\therefore i_1 > 0 \Rightarrow$ D is OFF.

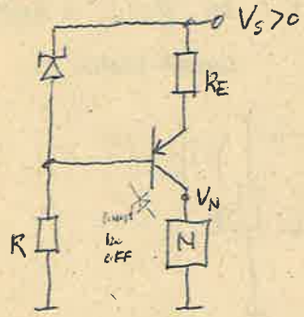
$$v_{out}(t) = V_R - \frac{1}{C}\int_{T_1}^{t} (\beta_F i_b - I)\,dt$$

$$= V_R - \frac{(\beta_F I_B - I)(t - T_1)}{C}$$

If $\beta_F i_b - I \gg I \Rightarrow$ sweep time $\gg$ recovery time

3003B2

Current Sources

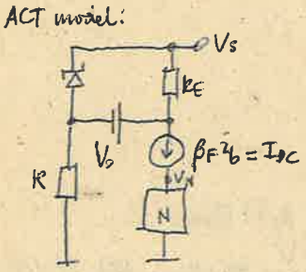


TR must be ACT $\Rightarrow$ BC diode must be OFF

$\Rightarrow V_N - (V_S - V_Z) < V_\gamma$

$$V_N < V_\gamma + V_S - V_Z$$

ACT model:

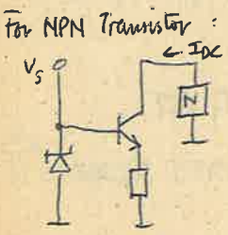


$$i_e = \frac{V_Z - V_\gamma}{R_E} \text{ constant}$$

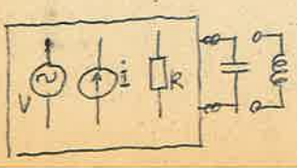
$$\beta_F i_b = \frac{\beta_F i_e}{\beta_F + 1} = \alpha_F i_e \cong i_e$$

$$I_{DC} = \frac{V_Z - V_\gamma}{R_E}$$

For NPN Transistor:



Networks Containing dependent Sources

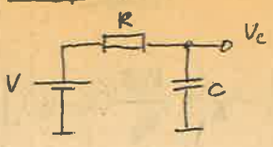


$$V = \sum_i a_i V_{ti} + \sum_i b_i i_{bi}$$

$a_i, b_i \rightarrow$ constants

$i_{bi} \rightarrow$ network currents

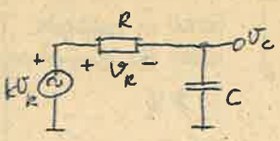
example:



$$C\frac{dv_c}{dt} = \frac{V - v_c}{R}$$

$$-\frac{dv_c}{dt} + \frac{v_c}{RC} = \frac{V}{RC}$$

$$v_c(t) = v_c(\infty) + [v_c(0) - v_c(\infty)]\,e^{-t/RC}$$



$$C\frac{dv_c}{dt} = \frac{kv_R - v_c}{R}$$

$$kv_R - v_R = v_c \Rightarrow v_R = \frac{v_c}{k-1}$$

$$C\frac{dv_c}{dt} = \frac{(kv_c/k-1) - v_c}{R}$$

$$C\frac{dv_c}{dt} = \frac{v_c}{(k-1)R} \Rightarrow \frac{dv_c}{dt} - \frac{v_c}{(k-1)RC} = 0$$

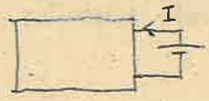
Solution: The waveforms are exponential.

Algorithm

(1) Find initial values by replacing the capacitor (inductor) by a constant voltage (current) source $V_c(0)$ ($i_L(0)$).

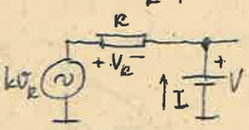
(2) Find steady-state values (i.e. $t = \infty$) by replacing the capacitor with an open circuit. (L → short circuit)

(3) Kill all independent sources. Remove C (or L) and replace it with a constant voltage source V. Find the current thru this voltage source. (I)



Evaluate $R_{TH} \triangleq \frac{V}{I}$ Then $\tau = R_{TH}C$

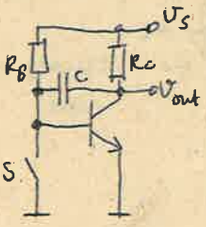
$$V_R(0) = \frac{V_c(0)}{k-1}$$



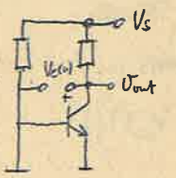
$$\left.\begin{aligned} V &= kv_R - v_R \\ v_R &= -RI \end{aligned}\right\} \quad V = -(k-1)RI$$

$$R_{TH} = \frac{V}{I} = -(k-1)R$$

Miller Sweep Generator:



At $t = 0^-$ switch is closed. The circuit is at S.S. ∴ C is open.

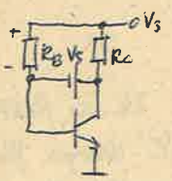


TR is OFF.

$v_o(0^-) = V_S$

$V_C(0^-) = V_S$

At $t = 0^+$ open the switch:



$V_{BC} = -V_S < V_\gamma$

$$V_{BE}(0^+) = V_S - \frac{V_S}{R_B + R_C} R_B > V_\gamma$$

has to be satisfied

$\Rightarrow$ TR is ACT

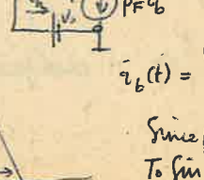
TR can't be SAT

$v_o(0^+) = V_C(0) + V_\gamma = V_S + V_\gamma$

$v_o(\infty) = V_S - R_C\beta_F i_b(\infty)$

$$v_o(\infty) = V_S - R_C\beta_F \frac{V_S - V_\gamma}{R_B} < 0$$

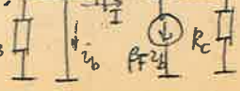
has to be satisfied



$$i_b(t) = \frac{V_S - V_\gamma}{R} + i_q(t) \quad \leftarrow \text{not constant}$$

Since $\beta_F i_b$ depends on i_q

To find τ:



$$V = R_C(I - \beta_F i_b)$$

$i_b = -I \Rightarrow V =$

$R_C(I + \beta_F$

$$R_{TH} = \frac{V}{I} = R_C(\beta_F +$$

For $0 \le t < T_S$

$$V_{out}(t) = V_S - \frac{R_C\beta}{R_B}(V_S - V_0) + \left[V_S + V_0 - V_B + \frac{R_C\beta}{R_B}(V_S - V_0)\right] e^{-t/\underbrace{R_C C(\beta+1)}_{\tau_1}}$$

$V_{out}(T_S) = 0$

$$T_S = \tau_1 \ln\left[1 - \frac{V_S + V_0}{\frac{R_C\beta}{R_B}(V_S - V_0) - V_S}\right]$$

× terms are considered as negligible under the assumptions:

$V_S \gg V_0$

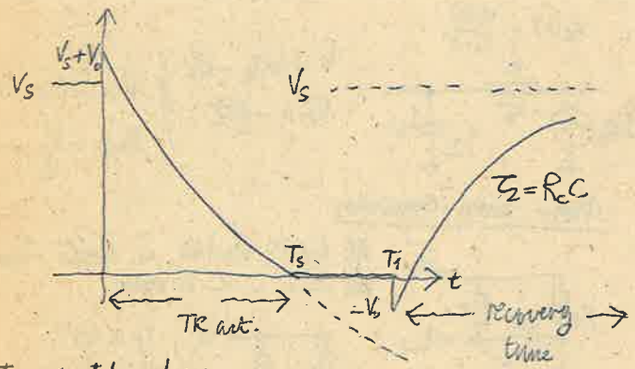
$\frac{R_C\beta}{R_B} \gg 1$

$$\simeq \tau_1 \ln\left[1 - \frac{1}{\frac{R_C\beta}{R_B}}\right] \simeq \frac{\tau_1 R_B}{R_C\beta}$$

$\frac{T_S}{\tau_1} = \frac{R_B}{R_C\beta} \ll 1 \Rightarrow$ sweep is almost linear.
(τ is much greater than sweep time)

$$T_S = \frac{R_C C(\beta+1) R_B}{R_C\beta}$$

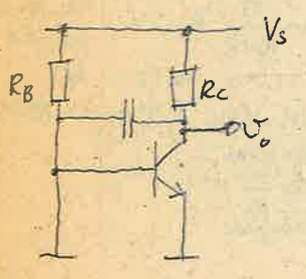
$$\simeq R_B C$$ if β is large, sweep time doesn't depend on transistor parameters.



At T_1 switch closes,

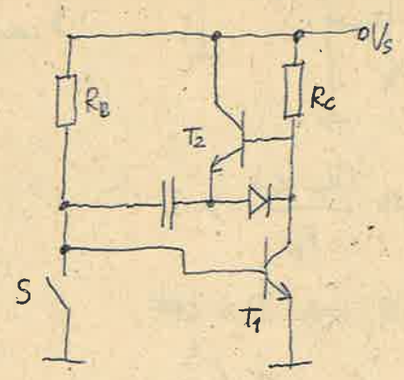
$V_C(T_S) = -V_0 = V_C(T_1)$

For $t \ge T_1$



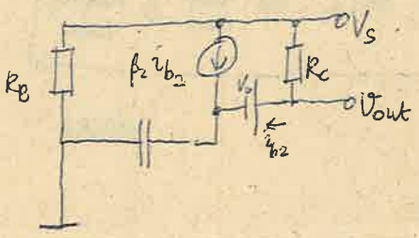
At $t = T_1^+$ TR is REVACT, but since 'C' charges through R_C and the switch TR will immediately be OFF.

recovery time must be very short, so a modification is required:



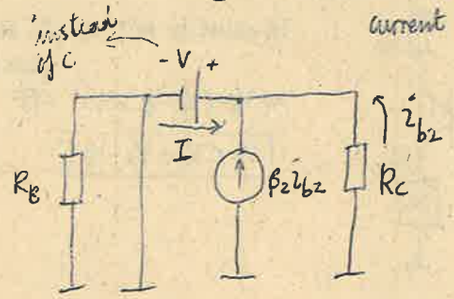
When S is closed, C charges through R_C, T_2 and the switch. BE junction of T_2 makes D OFF. T_2 is ACT, T_1 is OFF.

Model at recovery time:



$$i_{b_2}(t) = \frac{V_S - V_0 - V_C(t)}{R_C}$$

So $\beta_2 i_{b2}$ is dependent current source,



$V = -R_C i_{b2}$

$I = -(\beta_2+1) i_{b2}$

$R_{TH} \triangleq \frac{V}{I} = \frac{R_C}{\beta_2+1}$

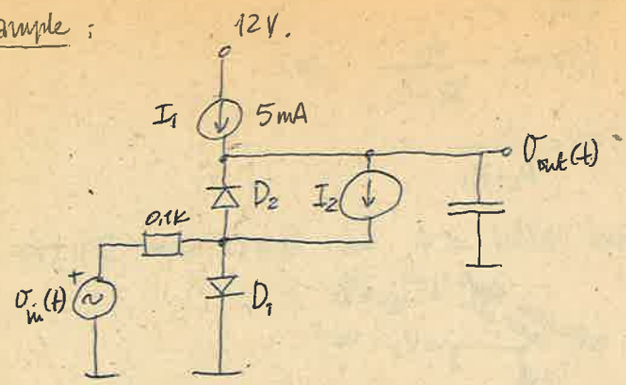
β_2+1 times smaller than old τ ($R_C C$)

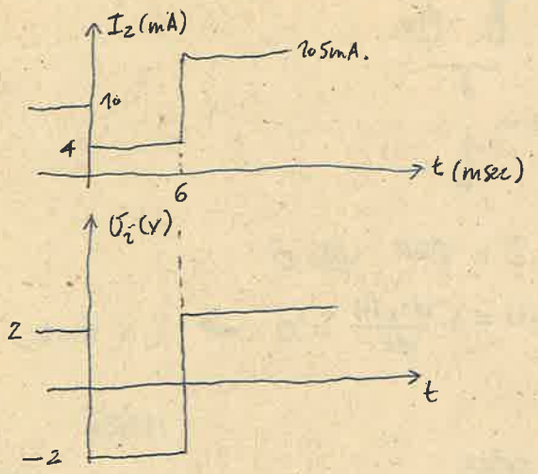
$$\tau = \frac{R_C C}{\beta_2+1}$$ ← this is

When S is open: D_1 is ON, T_2 OFF, T_1 ACT

↑ AT1 SUBJECTS

Example :



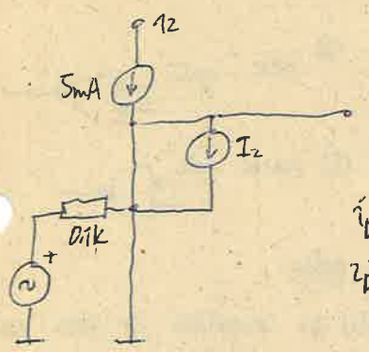


$t = 0^-$ C open.

$v_{in}(0^-) = 2\,V.$

$I_2 = 4\,mA.$

Assume D_1 ON, D_2 ON



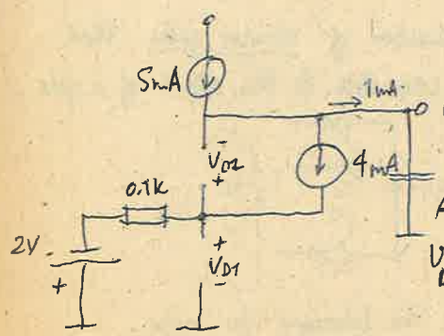
$i_{D2}(0^-) = 5\,mA > 0$ ✓

$i_{D1}(0^-) = I_2 - i_{D2}(0^-) + \frac{2}{0.1K}$

$= 25\,mA > 0$ ✓

$\therefore v_o(0^-) = v_c(0) = 0V.$

$t = 0^+$: $v_i = -2\,V.$, $I_2 = 4mA.$, $v_c(0) = 0\,V.$



Assume D_1 OFF, D_2 OFF

$V_{D1}(0^+) = -2 + (0.1k)(4mA)$

$= -1.6 < 0$ ✓

$V_{D2}(0^+) = V_{D1}(0^+) = -1.6\,V < 0$ ✓

$t > 0$:

$$v_o(t) = \frac{1}{C}\int_0^t 1\,mA\,d\tau = 10^3 t$$

$v_{D1}(t) = -1.6\,V.$ ⟶ D_1 always OFF

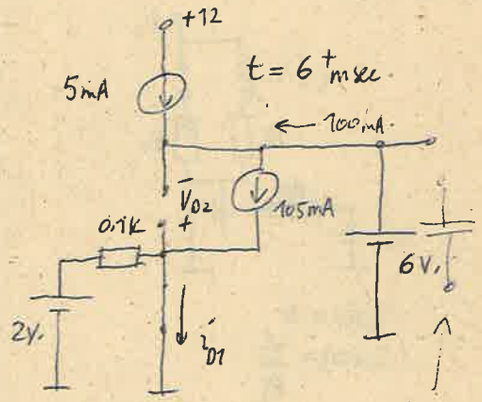
$V_{D2}(t) = -1.6 - v_o(t)$ ⟶ D_2 always OFF.

$v_o(6\,msec) = 6\,V. = v_c(6\,msec)$

$t = 6^+ msec$

$v_i = 2V.$

$I_2 = 105\,mA.$



Assume D_1 ON, D_2 OFF

$i_{D1}(6^+) = 105 + \frac{2}{0.1K}$

$= 125\,mA > 0$ ✓

$v_{D2}(6^+) = -6\,V < 0$ ✓

$t > 6$ msec

$$v_{out}(t) = 6 - \frac{1}{C}\int_{6ms}^t 100\,mA\,d\tau = 6 - 10^{+5}(t - 6\,msec)$$

$i_{D1}(t) = 125\,mA$ constant ⟹ always ON.

$v_{D2}(t) = -v_o(t)$

when $v_o(t) = 0$ D_2 will be ON

$v_o(t_1) = 0 = 6 - 10^5(t_1 - 6\,msec)$

$t_1 = 6^{msec}_{+} \frac{6}{10^5}\,sec = 6.06\,msec$

At $t = 6.06^+$ msec replace D_2 with short circuit and find the state of D_1 :

D_1 will be ON. (Show that it will not be OFF)

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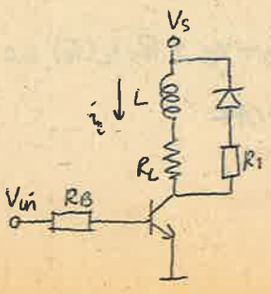
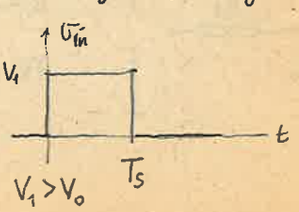
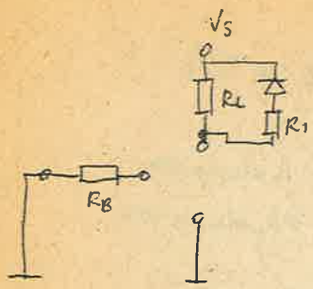
Current Sweep Generators



R_L : winding resistance of coil



At $t=0^-$: the circuit is at steady state $\therefore$ L is short

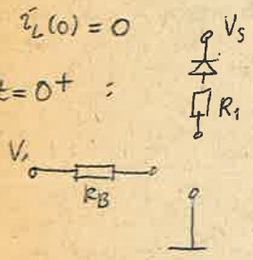


D is OFF.

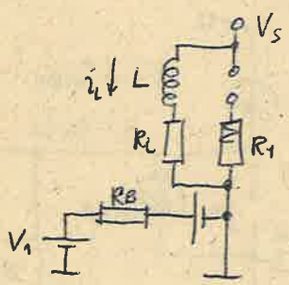
$\Rightarrow$ TR is OFF

$i_L(0) = 0$

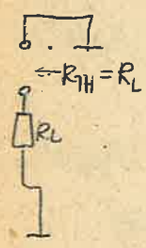
At $t=0^+$:



TR is SAT, at $t=0^+$;

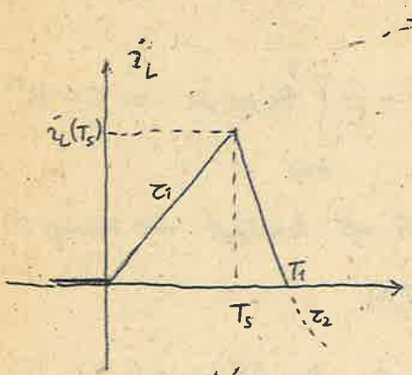


$\tau_1 = \frac{L}{R_L}$



$i_L(0) = 0$

$i_L(\infty) = \frac{V_S}{R_L}$



$$i_L(t) = \frac{V_S}{R_L} + \left[-\frac{V_S}{R_L}\right] e^{-t/\tau_1}$$

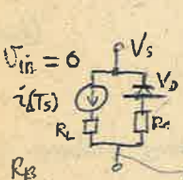
$$i_L(T_S) = \frac{V_S}{R_L}\left(1 - e^{-T_S/\tau_1}\right)$$

$\beta_F i_b > i_L(t)$ $\quad 0 < t < T_S$ $\leftarrow$ must be satisfied

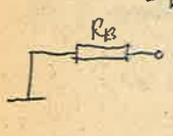
(i_b: constant)

$\boxed{\beta_F i_b > i_L(T_S)} \Rightarrow$ TR is SAT $\quad 0 < t < T_S$

$t = T_S^+$: $V_{in} = 0$



D is ON



$V_c = V_S + V_D + R_1 i_L(T_S) > 0$

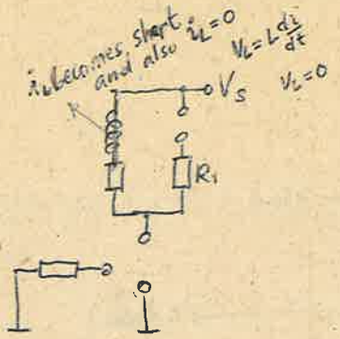
TR is OFF

$i_L(T_S)$:

$$i_L(\infty) = -\frac{V_D}{R_L + R_1} \quad (*)$$

$$\tau_2 = \frac{L}{R_L + R_1}$$

When $i_L(T_1) = 0 \Rightarrow i_D = 0 \Rightarrow$ D is OFF



When D is OFF $i_D(t) = 0$

$\therefore v_L(t) = L\frac{di_L(t)}{dt} = 0 \Rightarrow$ L is short.

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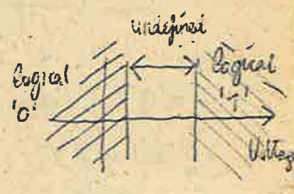
LOGIC GATES



We have two levels of signals.
- Logical '0' (low level 'L') signals
- " '1' high level 'H') signals

Symbols for gates :

① Inverter 

② OR gate 

③ AND gate 

④ NOR gate 

⑤ NAND gate 

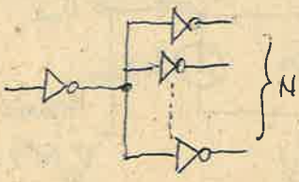
Specifications for logic gates

(1) Compatibility : Two gates are compatible if their voltage (or current) levels match.

Definitions : $V_{OL\,max}$ = max. output low level signal.

$V_{OH\,min}$ = min. output high level signal.

(2) Max. fan out : max. number of similar gates that can be connected to the output of a gate.



(3) Noise Margins : Gives the tolerance for noise.

LNM : "Low noise margin"

HNM "high noise margin"

(4) Power consumption : is important when the number of gates used are high.

Classification of integration :

(1) SSI "Small scale integration"
1 chip = max. 4 gate (20-40 components)

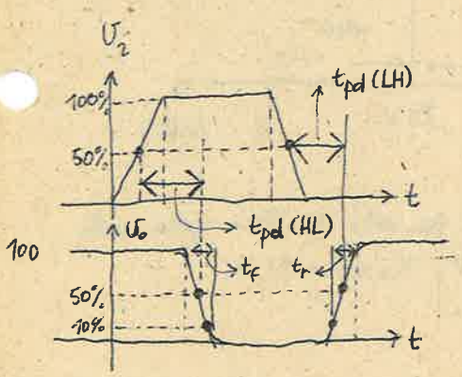
(2) MSI "Medium Scale integration"
1 chip = 20-40 gate (

(3) LSI "Large scale integration"
1 chip = 100-1000 gate

(4) VLSI "Very large scale integration"
1 chip → 200 000 TRansistors

(5) Power Supply : number and value of the power supply needed.

(6) Speed : max. attainable input frequency.



$t_{pd}(HL)$ propagation delay from high to low

$t_{pd}(LH)$: propagation delay from low to high

t_f : fall time
t_r : rise time

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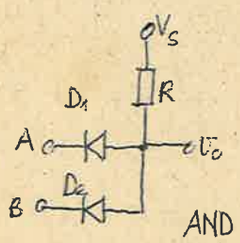
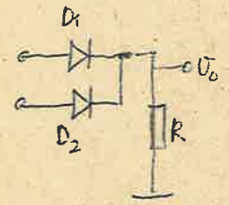
Diode Transistor Logic



AND Gate

A	B	D_1	D_2	U_0
H	H	OFF	OFF	H
H	L	OFF	ON	L
L	H	ON	OFF	L
L	L			L

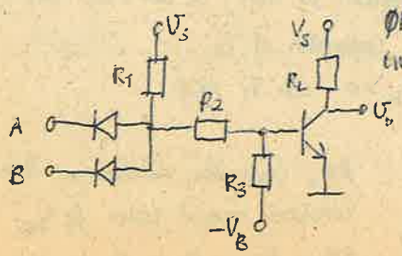
↓ the diode with the smallest input is ON the other is OFF



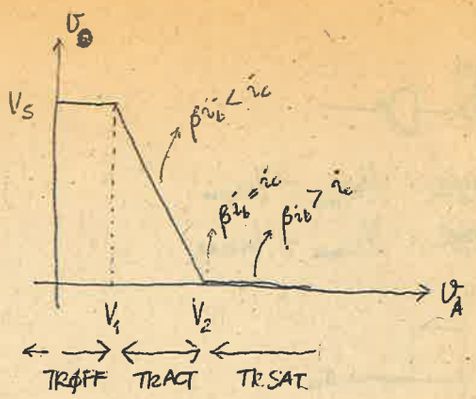
OR Gate

A	B	D_1	D_2	U_0
L	L	OFF	OFF	L
L	H	OFF	ON	H
H	L	ON	OFF	H
H	H			H

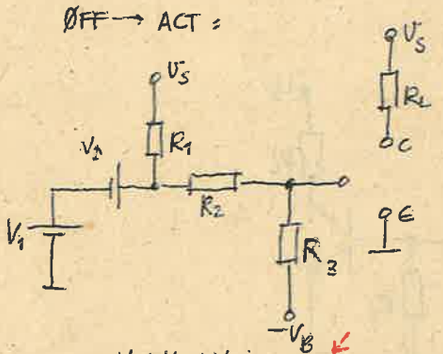
↓ the diode with largest input is ON, the other one is OFF



≡ NAND Gate



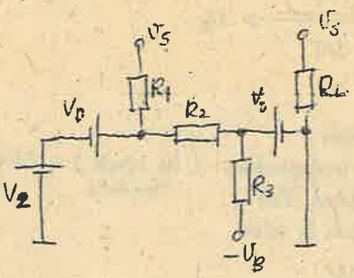
OFF → ACT :



$$U_{BE} = \frac{V_1 + V_D + V_B}{R_2 + R_3} \cdot R_3 - V_B = V_0$$

$$V_1 = \frac{R_2 + R_3}{R_3}(V_B + V_0) - V_B - V_D$$

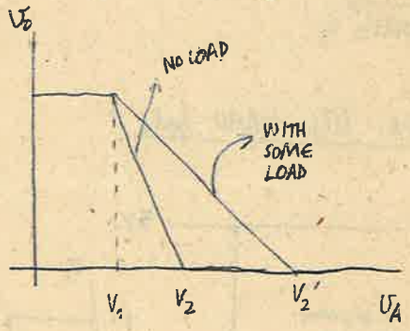
ACT → SAT :



$$i_{CSAT} = \frac{U_S}{R_L}$$

$$\beta i_b = \beta\left[\frac{V_2 + V_D - V_0}{R_2} - \frac{V_0 + V_B}{R_3}\right] = i_{CSAT}$$

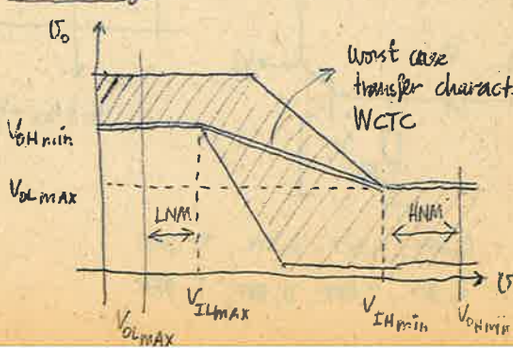
$$V_2 = \frac{R_2 i_{CSAT}}{\beta} + \frac{R_2(V_0 + V_B)}{R_3} - V_0 - V_D$$



with some load :

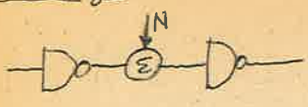
$$I_{CSAT} = NI_b + \frac{U_S}{R_L}$$

in catalogs :



must be :
$V_{OH\,min} > V_{IH\,min}$
$V_{OL\,max} < V_{IL\,max}$
for cascade connection

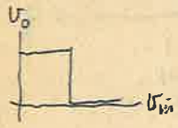
noise margin :



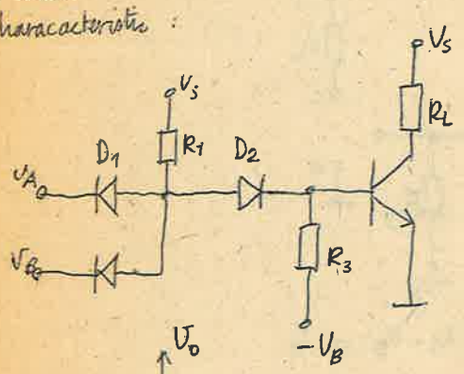
(HNM) High noise margin : $V_{OH_{min}} - V_{IH_{min}}$

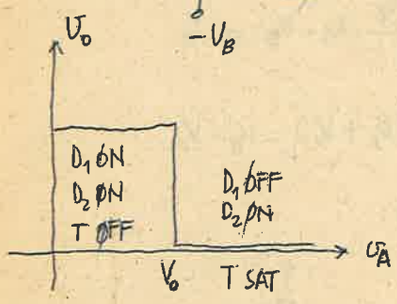
(LNM) Low noise margin : $V_{IL_{max}} - V_{OL_{max}}$

ideal gate characteristic :



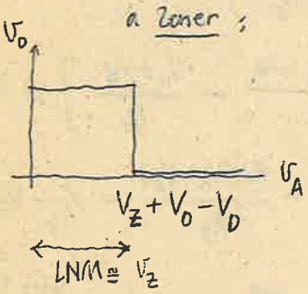
achievement to ideal characteristic :



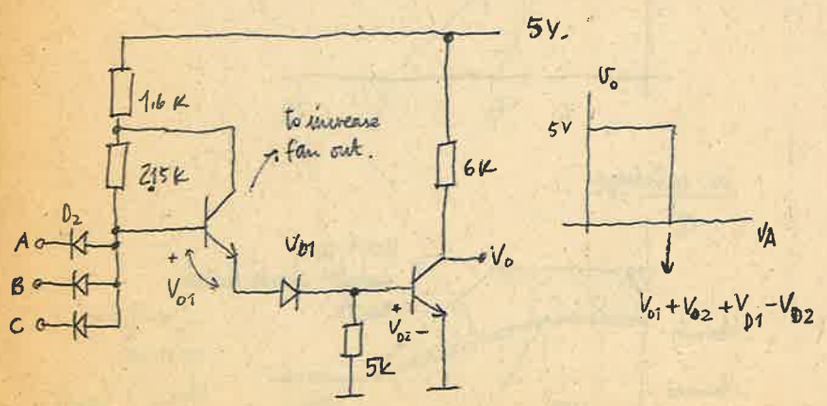


drawback of this configuration - (D_2 too small) $\simeq$ 0.6 V. threshold

To overcome this, substitute D_2 with a Zener :



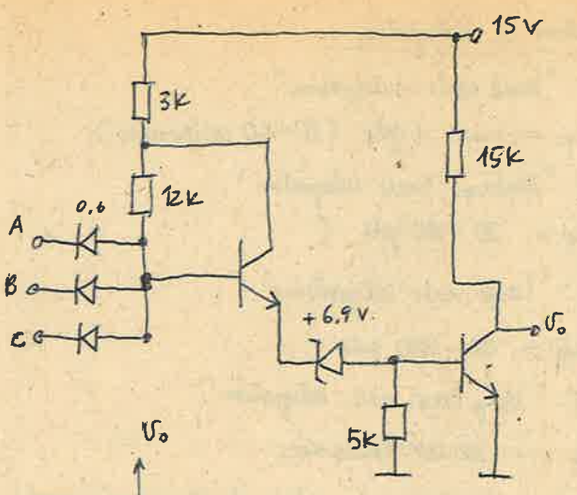
Integrated Circuit DTL NAND gate

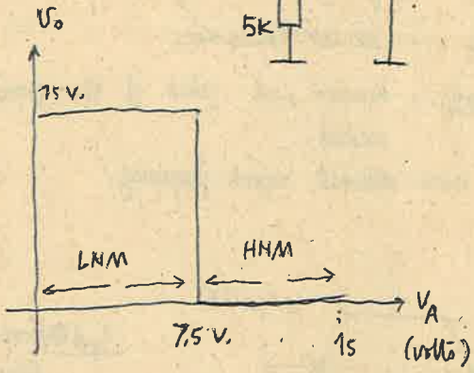


When input high : D_2 OFF, T_1 ACT, D_1 ON, T2 SAT

When input low : D_2 ON, T_1 OFF, D_1 OFF, T_2 OFF

High Threshold logic (HTL)

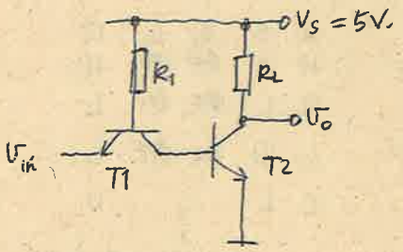




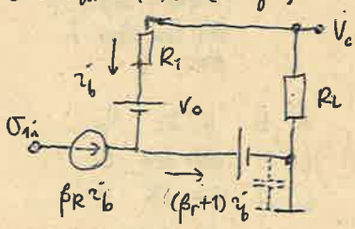
Exercise :

Obtain the max. fan outs of these gates with $\beta = 50$, $V_o = 0.6$ V, $V_{CESAT} = 0.2$ V.

Transistor - transistor logic (TTL)



Let $V_{in} = 4$ V. (high) : T_1 REVACT, T_2 SAT :

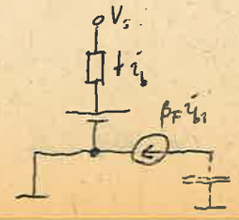


$\beta_r \cong 0.02$

$$i_b = \frac{V_S - 2V_o}{R_1} \simeq i_{b2}$$

When input is reduced to zero, T_1 can't be SAT, due to base-emitter capacitor of T_2. (T_2 ACT)

$V_{CE1} = 0.6$ V., $i_{b1} > 0 \Rightarrow T_1$ ACT



BE_2 capacitor discharges thru, constant current source $\beta_F i_{b2}$

When $V_{CE1} = 0$ V., T_1 becomes SAT

T_2 OFF

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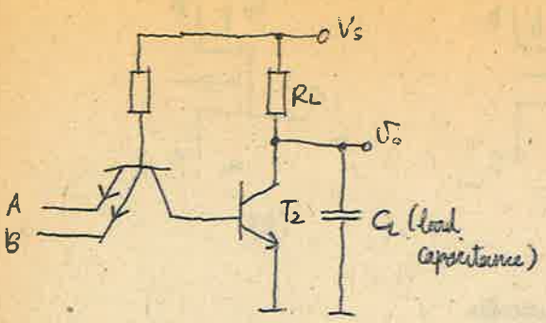
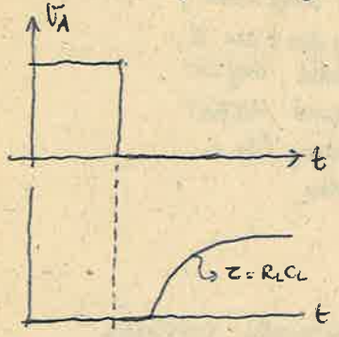


TR SAT $V_C = 0$ initially.

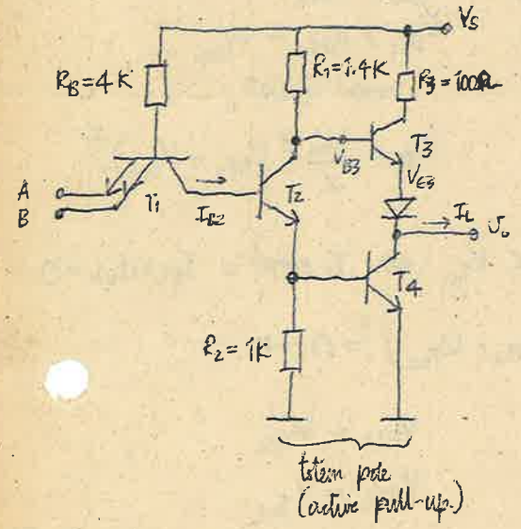
because of C, propagation delay (rise time) increase.

when T_2 OFF, C charges



To prevent that disadvantage, we put an emitter follower to the collector of T_2.

IC - TTL GATE



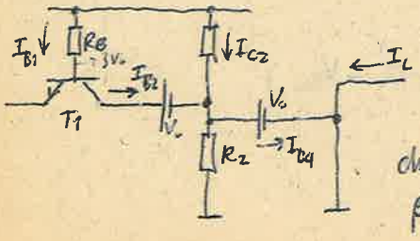
① A, B high ; T_1 REVACT, T_2 SAT, T_4 SAT, T_3 OFF, D OFF

$V_{E3} = V_{CESAT_4} + V_D$

$V_{B3} = V_{O4} + V_{CESAT_2}$

To have T_3 OFF, $V_{B3} < V_{E3} + V_{O3}$

$V_{O4} + V_{CESAT_2} < V_{CESAT_4} + V_D + V_{O3}$



$I_{B2} = (1+\beta_R) I_{B1}$ $\beta_R \cong 0.02$

$\cong I_{B1}$

To have T_2 SAT:

$\beta_2 I_{B2} > I_{C2} \Rightarrow \beta_2 I_{B1} > I_{C2}$

choosing β_2 properly, satisfy:

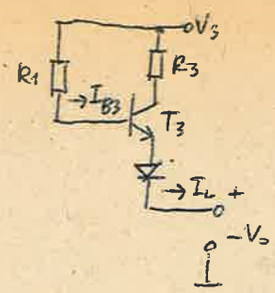
$$\beta_2 \frac{V_S - 3V_o}{R_B} > \frac{V_S - V_o}{R_1}$$

T_1 SAT: $\beta_4 (I_{C2} + I_{B2} - \frac{V_o}{R_2}) > I_L$

$\beta_4 (\frac{V_S - V_o}{R_1} + I_{B1} - \frac{V_o}{R_2}) > I_L$

$N \cong 10 \Rightarrow 16\,mA$ sink current for $16\,mA$.

② A and/or B are low T_1 SAT, T_2 OFF, T_4 OFF, T_3 ACT, D ON

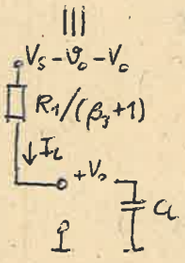


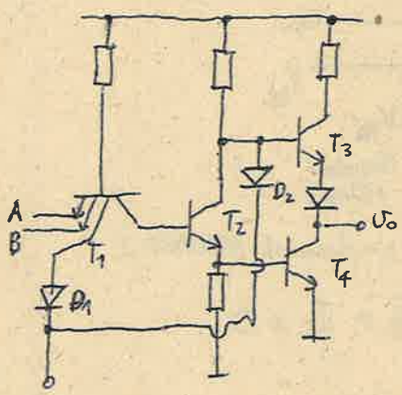
$$I_{B_3} = \frac{V_S - V_o - V_D - V_o}{R_1}$$

$I_L = (\beta_3 + 1) I_{B_3}$ (because T_3 ACT)

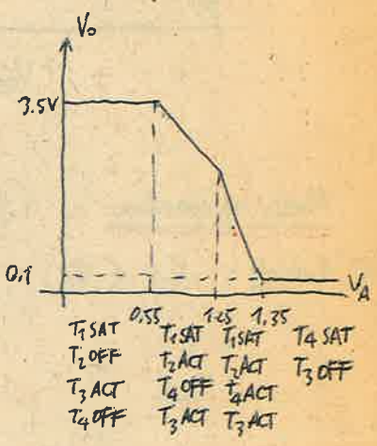
$$= \frac{\beta_3 + 1}{R_1} (V_S - V_o - V_D - V_o)$$

$$\tau = \frac{R_1 C_L}{\beta_3 + 1}$$





Tri-state stage.



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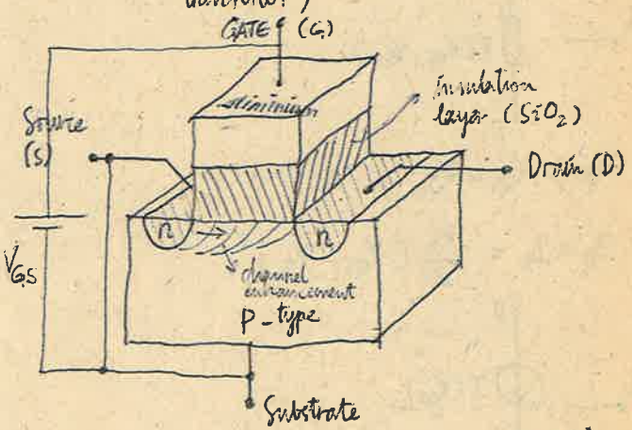
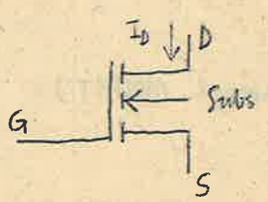
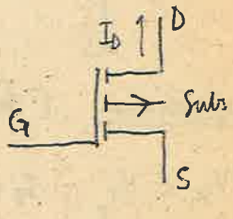
CMOS logic family :

MOSFET (Metal Oxide Semiconductor field effect Transistor)



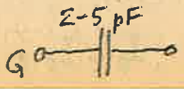


n - type

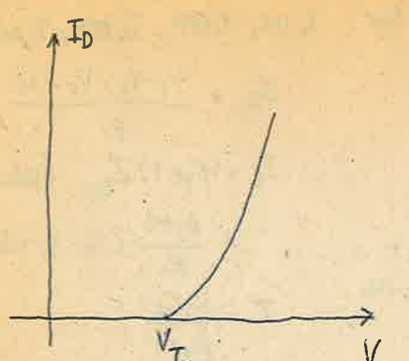


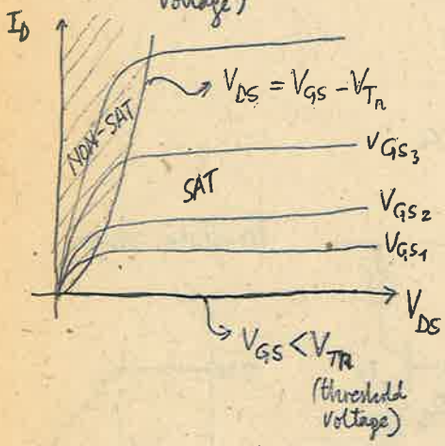
p - type

between Gate and Substrate, there is a capacitor (Due to insulator) $\Sigma = 5\,pF$



$\Rightarrow$ DC gate current is zero.



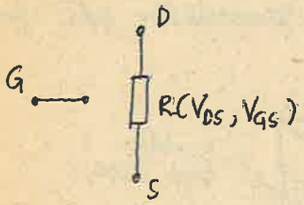


Modes of operation : (for n-channel MOSFET)

(1) Cut off : $V_{GS} < V_{Tn}$, $I_D = I_S = 0$

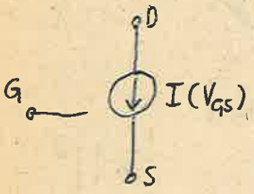
(2) Non-Sat : $V_{DS} \leq V_{GS} - V_{Tn}$

$$I_D = I_S = K_n\left[(V_{GS} - V_{Tn})V_{DS} - \frac{V_{DS}^2}{2}\right]$$



(3) Sat : $V_{DS} > V_{GS} - V_{Tn}$

$$I_D = I_S = \frac{K_n}{2}(V_{GS} - V_{Tn})^2$$



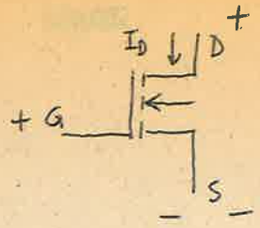
Modes of operation (for p-channel MOSFET)

(1) Cut off : $V_{SG} < V_{Tp}$, $I_D = I_S = 0$

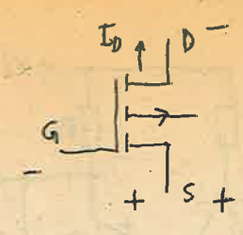
(2) Non-Sat $V_{SD} \leq V_{SG} - V_{Tp}$

$$I_D = I_S = K_n\left[(V_{SG} - V_{Tp})V_{SD} - \frac{V_{SD}^2}{2}\right]$$

(3) Sat $V_{SD} > V_{SG} - V_{Tp}$ $I_D = I_S = \frac{K_p}{2}(V_{SG} - V_{Tp})^2$

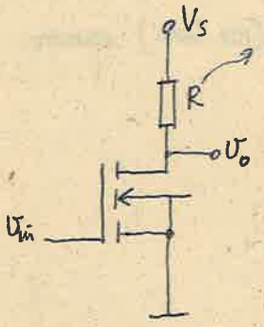


(n)

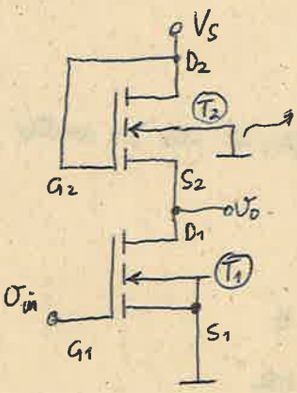


(p)

MOSFET inverter :



since Resistors in IC's covers very large area; they don't use R, instead, they use a second MOSFET behaving like a resistor.



generally, substrates are connected to smallest voltage level in the circuit (for n-type)

for p type : greatest voltage level.

$V_{GS_2} = V_{DS_2}$

$V_{DS_2} > V_{GS_2} - V_{Tn_2}$

$\Rightarrow$ T_2 SAT.

$$I_{D2} = \frac{K_{n2}}{2}(V_{GS_2} - V_{Tn_2})^2$$

(1) $U_{in} = V_{GS_1} < V_{Tn_1} \Rightarrow T_1$ OFF $= I_{D1} = I_{D2} = 0$

$$I_{D2} = \frac{K_{n2}}{2}(V_{GS_2} - V_{Tn_2})^2 = 0 \Rightarrow$$

$V_{GS_2} = V_{Tn_2}$

$V_{DS_2} = V_{Tn_2}$

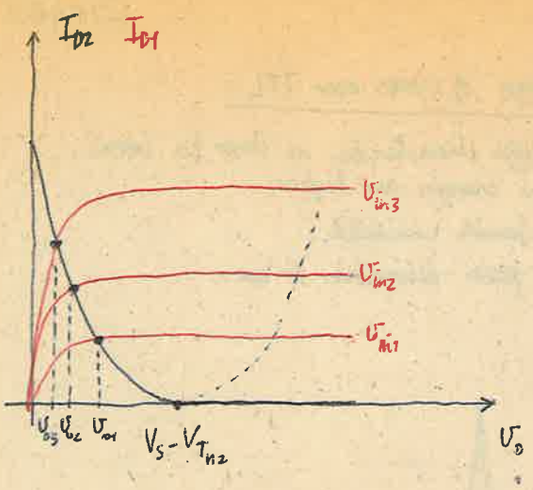
$\therefore U_o = V_S - V_{DS_2}$

$= V_S - V_{Tn_2}$

(2) $U_{in} > V_{Tn_1}$

$$I_{D2} = \frac{K_{n2}}{2}(V_{GS_2} - V_{Tn_2})^2 = \frac{K_{n2}}{2}(V_{DS_2} - V_{Tn_2})^2$$

$$= \frac{K_{n2}}{2}(U_S - U_o - V_{Tn_2})^2$$

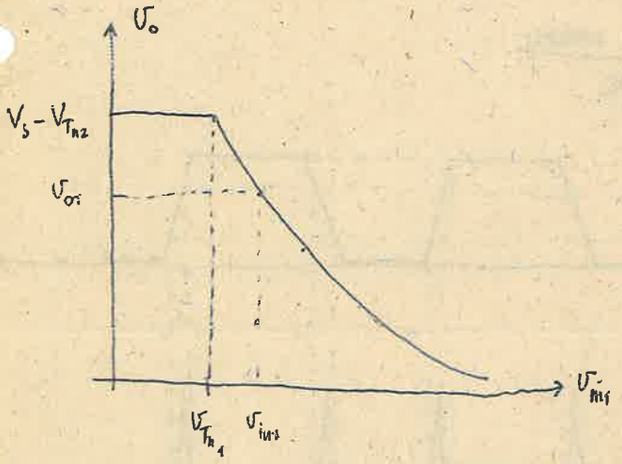


if $V_o > V_S - V_{Tn2}$,

$V_{DS_2} = V_S - V_o$

$\therefore V_{DS_2} < V_S - (V_S - V_{Tn2}) = V_{Tn2}$

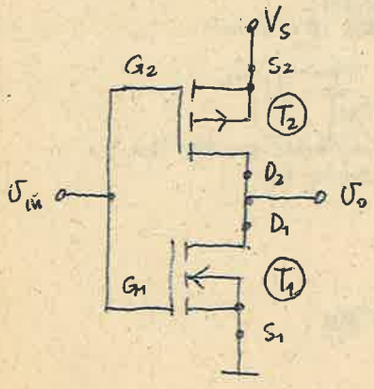
$V_{GS_2} < V_{Tn2} \Rightarrow T_2$ OFF $\therefore I_{D2} = 0$



" For better V_o-V_{in} characteristic, choose $\frac{K_{n2}}{K_{n1}}$ as small as possible "

To reduce power dissipation, they use complementary MOSFET's :

CMOS inverter

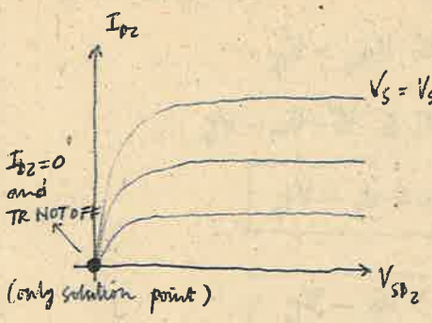


(1) $V_{in} = 0$ $\quad V_{in} = V_{GS_1} < V_{Tn} \Rightarrow T_1$ OFF

$\therefore I_{D1} = 0$

$I_{D2} = 0$

$V_{SG_2} = V_S - V_{in} = V_S > V_{Tp}$ → SAT / NON SAT



$\therefore V_{SD_2} = 0$

$V_o = V_S - V_{SD2}$

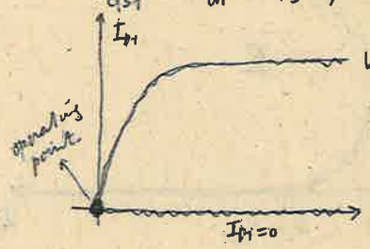
$\boxed{V_o = V_S}$

(2) $V_{in} = V_S$

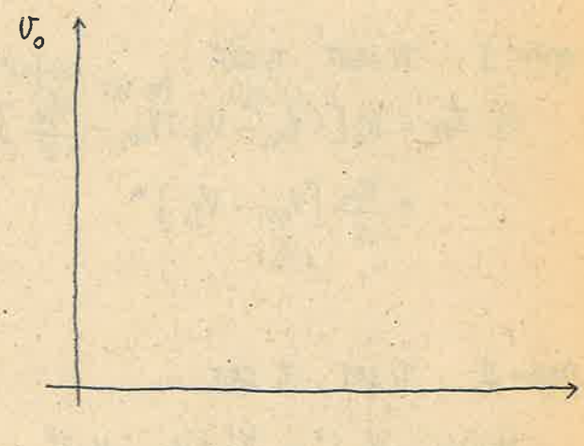
$V_{SG_2} = V_S - V_{in} = 0 < V_{Tp} \Rightarrow T_2$ OFF.

$I_{D2} = I_{D1} = 0$

$V_{GS_1} = V_{in} = V_S > V_{Tn} \Rightarrow T_1$ NOT OFF → SAT / NONSAT



$\therefore V_{DS1} = 0 = \boxed{V_o = 0}$



For $V_{in} = 0$, T_1 is OFF I_D is zero

" $V_{in} = V_S$, T_2 is OFF "

$\therefore$ DC power dissipation is zero.

$V_{in} = V_{GS_1}$ $\quad V_o = V_{DS_1}$

$V_{in} = V_S - V_{SG_2}$ $\quad V_o = V_S - V_{SD_2}$

for T_1 OFF : $V_{in} < V_{Tn}$

" T_1 NSAT : $V_{DS_1} \leq V_{GS_1} - V_{Tn}$

$V_o \leq V_{in} - V_{Tn}$

$\boxed{V_{in} \geq V_o + V_{Tn}}$

for T_1 SAT : $V_{in} < V_o + V_{Tn}$

for T_2 OFF : $V_{SG_2} < V_{Tp}$

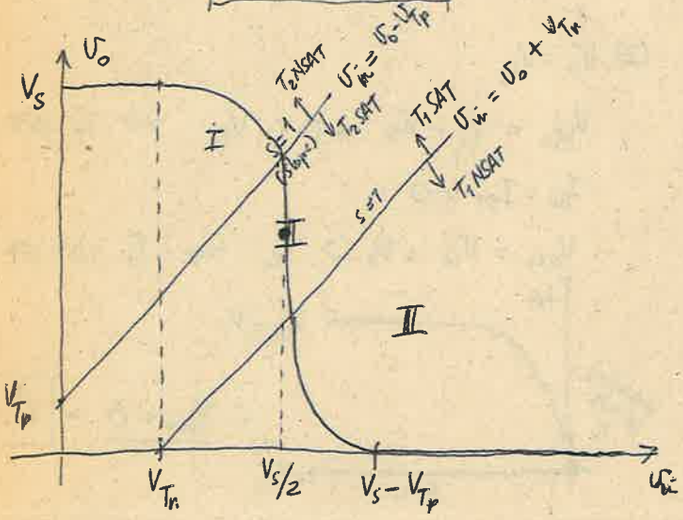
$V_s - V_{in} < V_{Tp} \Rightarrow \boxed{V_{in} > V_s - V_{Tp}}$

for T_2 NSAT : $V_{SD_2} \leq V_{SG_2} - V_{Tp}$

$V_s - V_o \leq V_s - V_{in} - V_{Tp}$

$\boxed{V_{in} \leq V_o - V_{Tp}}$

for T_2 SAT : $\boxed{V_{in} > V_o - V_{Tp}}$



in region I : T_2 NSAT , T_1 SAT

$$I_{D2} = K_p\left[(V_{SG_2} - V_{Tp})V_{SD_2} - \frac{V_{SD_2}^2}{2}\right]$$

$(V_s - V_{in})$ $(V_s - V_o)$ $(V_s - V_o)^2$

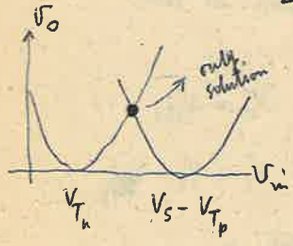
$$= \frac{K_{n_2}}{2}\left[V_{GS_1} - V_{Tn}\right]^2$$

(V_{in})

region II : T_1 SAT , T_2 SAT :

$$\frac{K_p}{2}(V_{SG_2} - V_{Tp})^2 = \frac{K_n}{2}(V_{GS_1} - V_{Tn})^2$$

$$\frac{K_p}{2}(V_s - V_{in} - V_{Tp})^2 = \frac{K_n}{2}(V_{in} - V_{Tn})^2$$



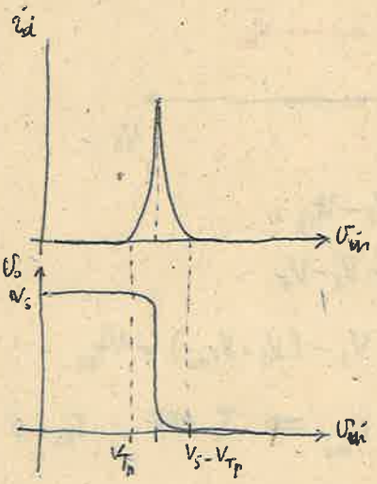
$$\sqrt{K_p}(V_s - V_{in} - V_{Tp}) = \sqrt{K_n}(V_{in} - V_{Tn})$$

$$V_{in} = \frac{\sqrt{K_p}V_s - \sqrt{K_p}V_{in} + \sqrt{K_n}V_{Tn}}{\sqrt{K_n} + \sqrt{K_p}}$$

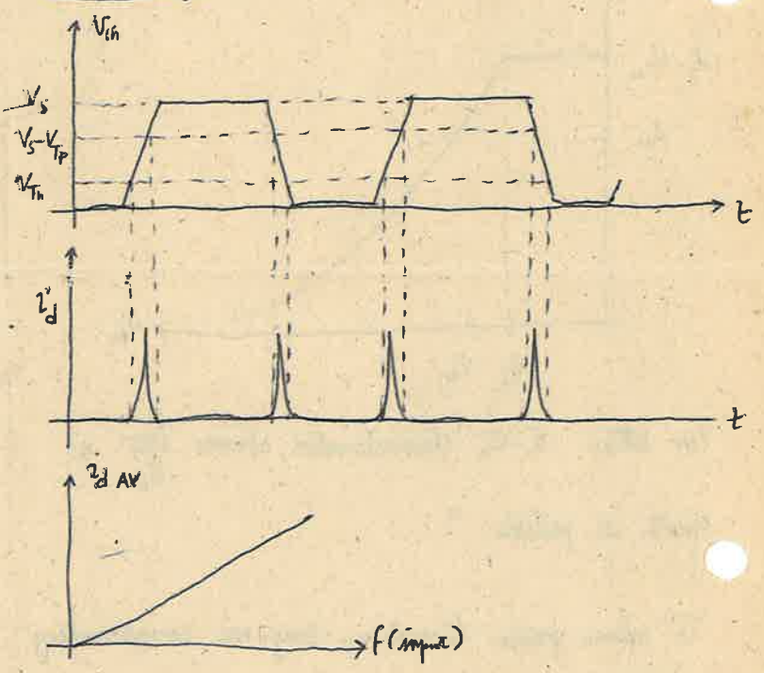
if $V_{Tn} = V_{Tp}$, $K_n = K_p \Rightarrow V_{in} = \frac{V_s}{2}$

Advantages of CMOS over TTL :

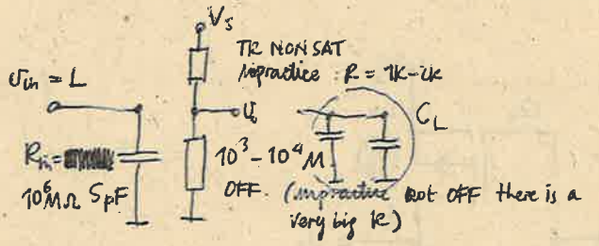
1. Transfer characteristic is closer to ideal.
2. Noise margins are higher.
3. DC fanout unlimited.
4. DC power dissipation is zero.

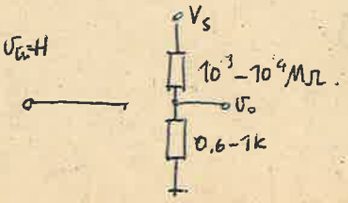


AC working :



∴ Average dissipated power increases with increasing input frequency.



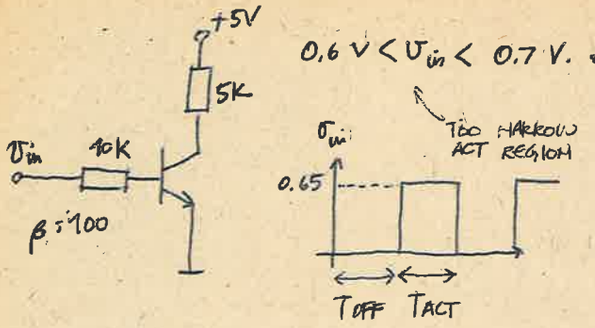


P_{AV} dissipated $= C_L V_s^2 f$ ∴ 1. AC fanout limited

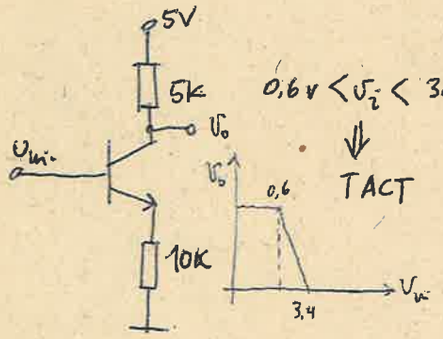
2. Input frequency limited

$V_{BG\,SUBS} \cong 100\ V.$

EMITTER_COUPLED LOGIC (ECL)



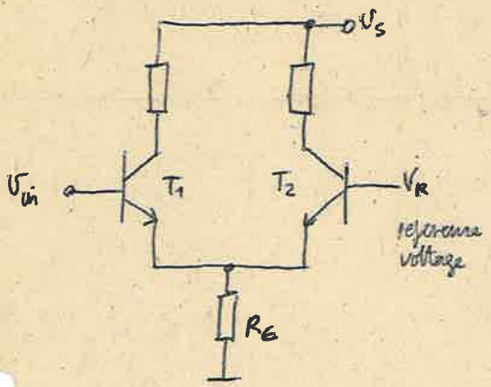
$0.6\ V < V_{in} < 0.7\ V. \Rightarrow T_{ACT},$



$0,6\ V < V_i < 3,4\ V.$

$\Downarrow$

T_{ACT}



$V_i > V_R \Rightarrow T_1$ ACT, T_2 OFF

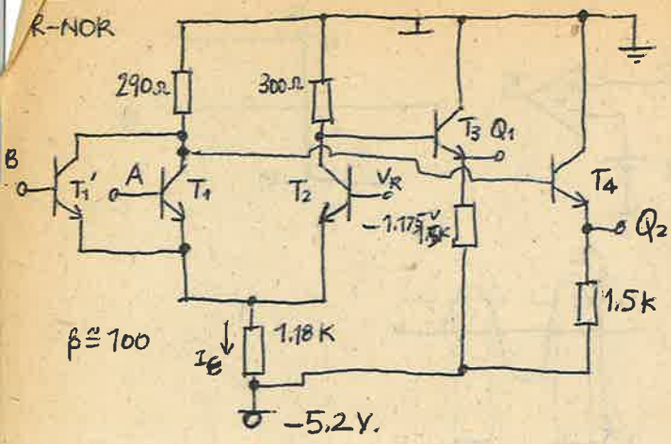
$V_i < V_R \Rightarrow T_1$ OFF, T_2 ACT

ECL

300482

Motorola

R-NOR



A·B	T_1'	T_1	T_2	T_3	T_4	Q_1	Q_2
L L	OFF	OFF	ACT			L	H
L H	ACT	OFF	OFF			H	L
H L	OFF	ACT	OFF			H	L
H H	ACT	ACT	ACT	ACT		H	L
						OR	NOR

Transfer characteristics :

OR ; v_{Q1} vs. v_A

T_1 ACT, T_2 OFF

$v_A = H > -1.175\,v$.

Assume $i_{b_3} = 0 \Rightarrow v_{b_3} = 0\,v. \Rightarrow v_{Q_1} = -0.6\,v.$

$i_{e_3} = (-0.6 + 5.2)/1.5K = \frac{4.6}{1.5} = 3.087$ mA.

$\Rightarrow i_{b_3}' = \frac{3.08}{101} = 0.031$ mA.

$v_{B_3} \cong 0.3K \cdot 0.03mA = 0.009\,v.$

$v_{Q_1} = -0.609 \cong -0.61V.$

$v_A = L < -1.175$ T_1 OFF T_2 ACT.

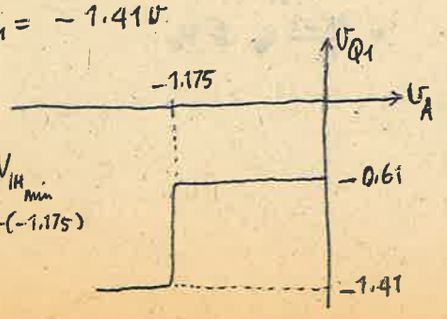
$I_E = \frac{-1.175 - 0.6 + 5.2}{1.18} \cong 2.9$ mA.

$i_{C_2}' \cong 2.9$ mA.

Assume $i_{b_3}' = 0$.

$v_{B_3} = -(0.3K)(2.9mA) = -0.81\,v.$

$v_{Q_1} = -1.41\,v$



$H_{NM} = V_{OH_{min}} - V_{IH_{min}}$

$= -0.61 - (-1.175)$

$= 0.5\,v.$

$L_{NM} = V_{IL_{max}} - V_{OL_{max}}$

$= -1.17 - (1.41)$

$= -0.3\,V.$

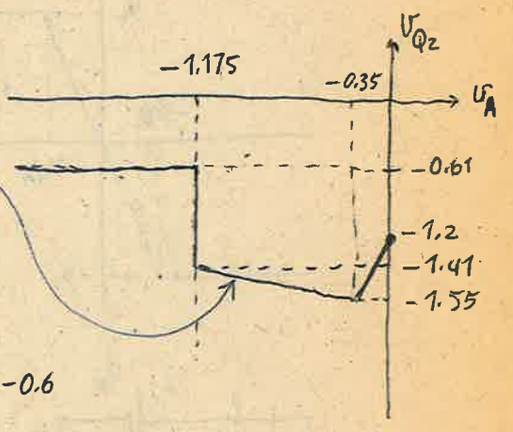
NOR : v_{Q2} vs v_A

$v_A = L$ T_1 OFF, T_2 ACT

Assume $v_{B4} = 0 \Rightarrow v_{Q_2} = -0.6\,v$ $v_{Q_2} \cong 0.61\,v.$

$v_{B_4} = -\frac{290}{1180} v_A$

$v_{Q_2} \cong -\frac{290}{1180} v_A$



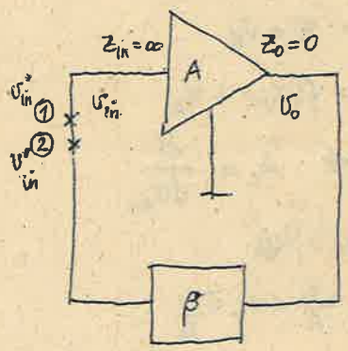
when $v_A \cong -0.35\,v$

T_1 is SAT.

$v_{Q_2} = v_A - 0.6 - 0.6$

REGENERATIVE CIRCUITS.

are circuits in which there is a positive feedback and the loop gain is greater than unity.



$v_o = A v_{in}$

$v_{in}' = \beta v_o$

$v_{in}'' = A\beta v_{in}$

$A_L = A\beta$

$\beta > 0$

Loop gain (A_L) = is the incremental gain from ① to ②

$A_L = \frac{dv_{in}'}{dv_{in}}$

For some time "t_1" let $v_{in} = V_1 \Rightarrow v_o = AV_1$

$v_{in}' = A\beta V_1 \Rightarrow v_o = A^2\beta V_1$

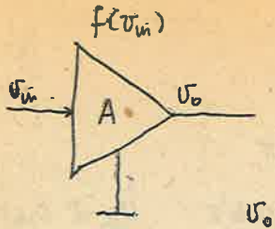
$v_{in}'' = A^2\beta^2 V_1 \ldots$

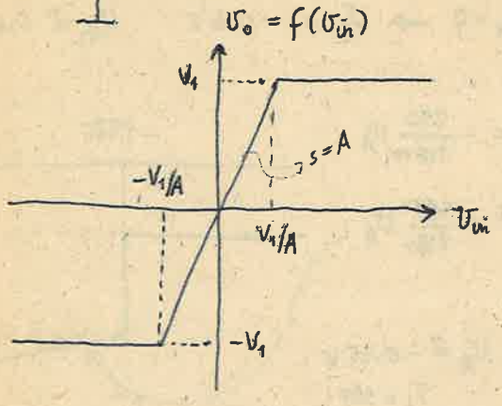
Case1 : $A\beta > 1 \Rightarrow v_o$ and v_{in} increases

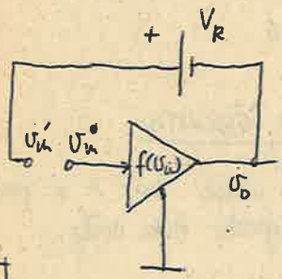
$\therefore$ the circuit is unstable.

Case2 $A\beta < 1 \Rightarrow v_o = v_{in} = 0$

$\therefore$ the circuit is stable.







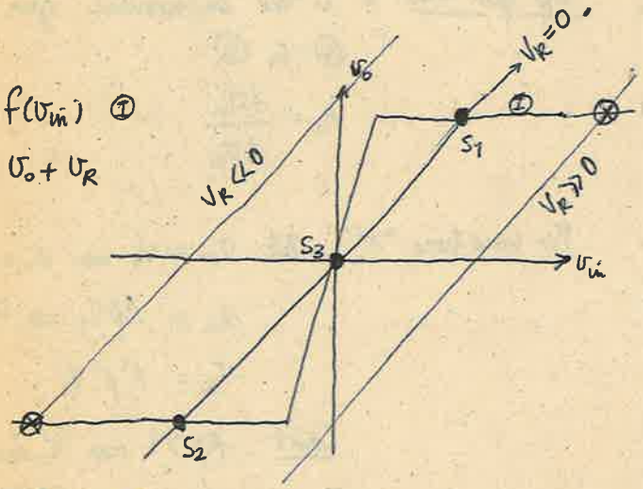
$$A_L = \frac{dv_{in}'}{dv_{in}}$$

$$v_{in}' = v_o + V_R$$
$$= f(v_{in}) + V_R$$
$$\Rightarrow A_L = \frac{df}{dv_{in}}$$

$$A_L = \begin{cases} 0 & \text{for } v_{in} > V_1/A \\ A \gg 1 & \text{for } \frac{-V_1}{A} < v_{in} < \frac{V_1}{A} \\ 0 & \text{for } v_{in} < -\frac{V_1}{A} \end{cases}$$

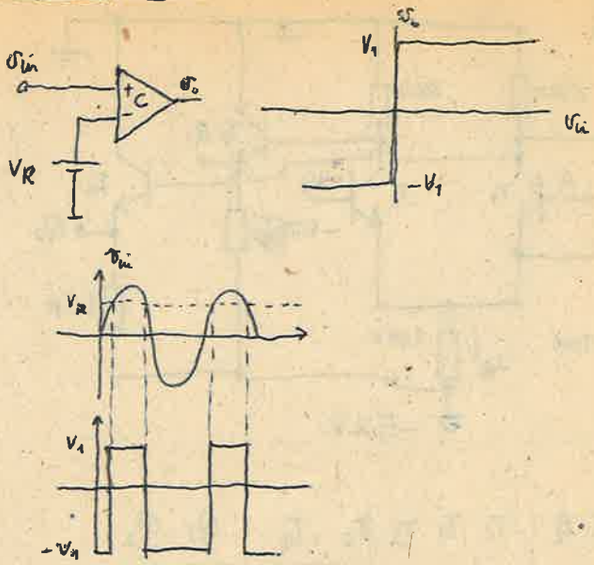
$v_o = f(v_{in})$ ①

$v_{in} = v_o + v_R$



Since at S_1 and S_2 the loop gain is less than unity, S_1 and S_2 are stable solutions. But at S_3 the loop gain is greater than one, therefore S_3 is an unstable solution.

Voltage comparator:



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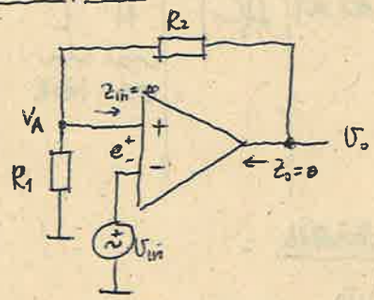
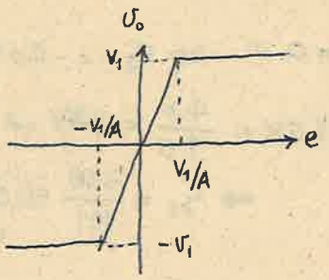
Regenerative Comparator





$$V_A = \frac{v_o R_1}{R_1 + R_2}$$

Since v_o is bounded V_A is also bounded.

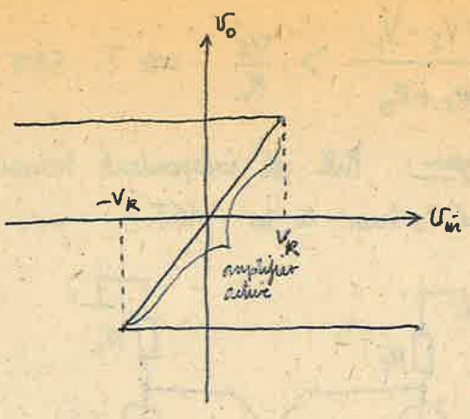
Assume $v_{in} = -\infty \Rightarrow e = \infty \Rightarrow v_o = V_1 \Rightarrow V_A = \frac{V_1 R_1}{R_1 + R_2}$

Increase $v_{in} \Rightarrow e$ decreases.

$v_o = V_1$ until 'e' becomes V_1/A

$$e = V_A - v_{in} = \underbrace{\frac{V_1 R_1}{R_1 + R_2}}_{\triangleq K} - v_{in} = \frac{V_1}{A}$$

$$v_{in} = KV_1 - \frac{V_1}{A}$$
$$= \frac{AK - 1}{A} v_o \triangleq V_R$$



Assume $v_{in} = \infty \Rightarrow e = -\infty \Rightarrow v_o = -V_1$

$$v_A = \frac{-V_1 R_1}{R_1 + R_2}$$

Decrease $v_{in} \Rightarrow e$ increases

$v_o = -V_1$ for $e < -V_1/A$

$$e = v_A - v_{in} = \underbrace{\frac{-V_1 R_1}{R_1+R_2}}_{\cong K} - v_{in} = -\frac{V_1}{A}$$

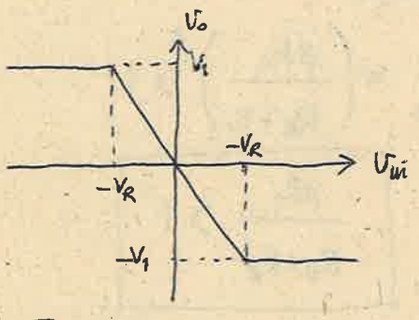
$$v_{in} = -\frac{(AK-1)}{A} V_1 \triangleq -V_R$$

For $-\frac{V_1}{A} < e < \frac{V_1}{A}$ Amplifier is Active

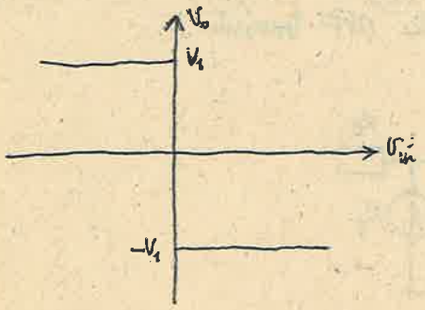
$$v_o = A(v_A - v_{in}) = A\left(\frac{v_o R_1}{R_1+R_2} - v_{in}\right)$$

$$V_R = \frac{(AK-1)V_1}{A}$$

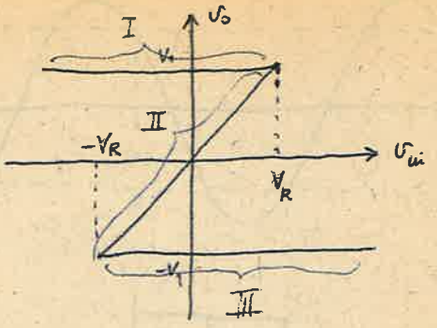
Case I $AK < 1$



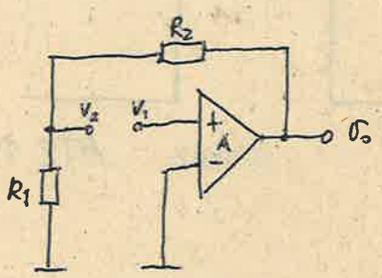
Case II $AK = 1$



Case III $AK > 1$



Loop gain ? :

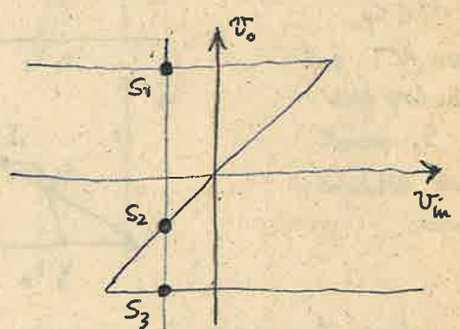


$$A_L \triangleq \frac{dV_2}{dV_1}$$

$$V_2 = \frac{R_1}{R_1+R_2} v_o = \frac{R_1 A V_1}{R_1+R_2}$$

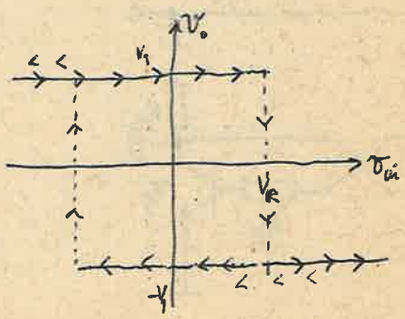
$$A_L = \frac{R_1 A}{R_1+R_2} = AK$$

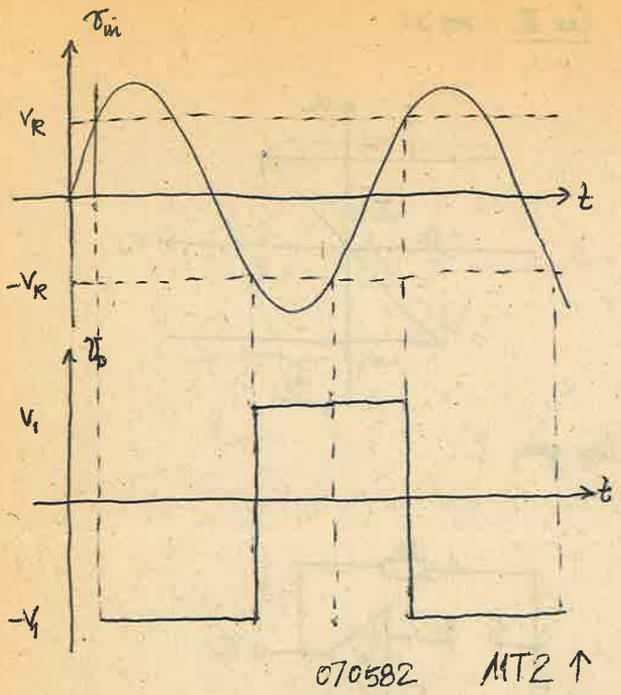
In Region I and III $A_L = 0$, in region II $A_L = AK \gg 1$



For $-V_R < v_{in} < V_R$ we have 2 stable outputs (S_1 and S_3) and one unstable output (S_2)

for $AK > 1$:





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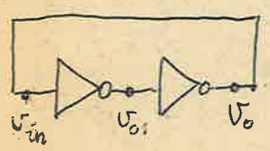
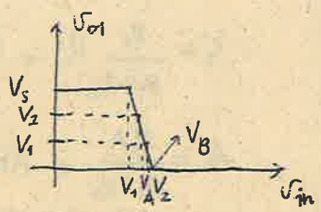
Bistable Multivibrator :

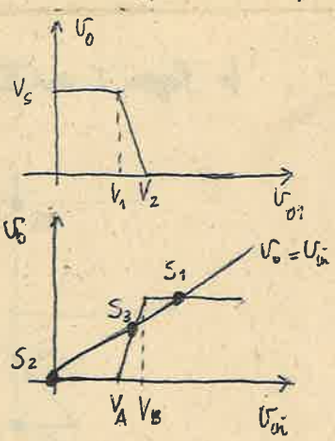
is a closed loop regenerative system having two stable states.

example :





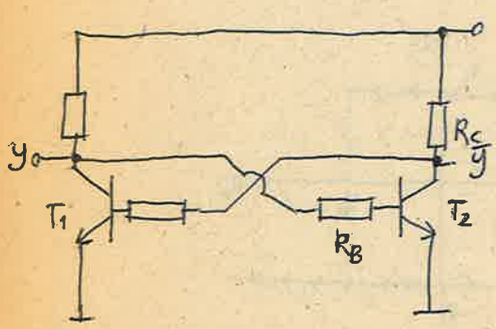
$v_o = v_{in}$



Since for $V_A < v_i < V_B$ both inverters are ACT, and assuming that the loop gain greater than one. S_3 cannot be stable solution. We have two stable solutions.

To switch the output from S_1 to S_2, we need some external force. This action is called triggering.

discrete bistable multivibrator (two transistor inverters)



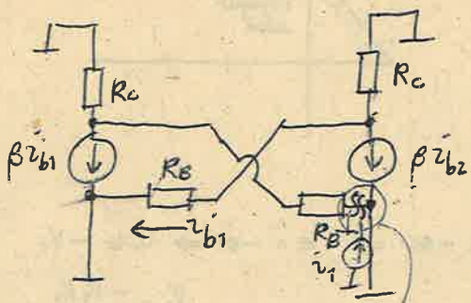
We must have 2 stable states and $A_L > 1$

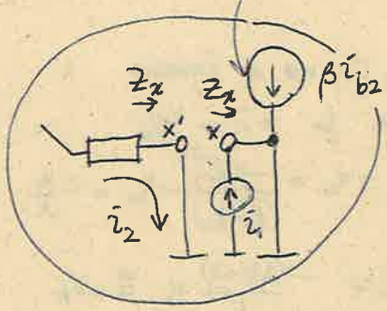
Stable states : 1) T_1 OFF, T_2 SAT

2) T_1 SAT, T_2 OFF

$$\frac{\beta (V_S - V_o)}{R_C + R_B} > \frac{V_S}{R_C} \Rightarrow T \text{ SAT}$$

Loop gain : Kill all independent sources (DC)
T_1 and T_2 have to be ACT.





① Measure Z_x (impedance at x)
② Terminate x_1 with Z_x

$$i_1 = i_{b2}$$

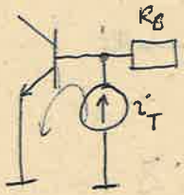
$$i_{b1} = -\frac{\beta i_1 R_C}{R_B + R_C}$$

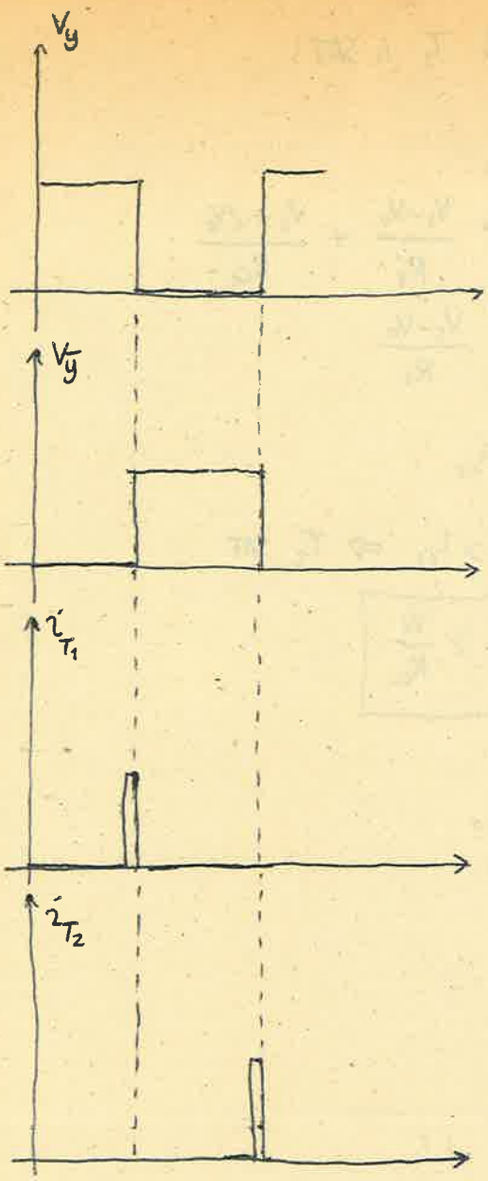
$$i_2 = \frac{\beta^2 R_C^2 i_1}{(R_B + R_C)^2}$$

$$A_L = \frac{di_2}{di_1} = \left(\frac{\beta R_C}{R_B + R_C}\right)^2 > 1$$

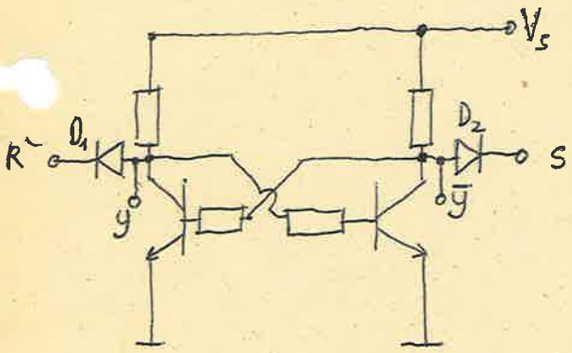
$$\boxed{\frac{\beta R_C}{R_B + R_E} > 1}$$

Triggering : Apply current pulses to the base of the OFF transistor.





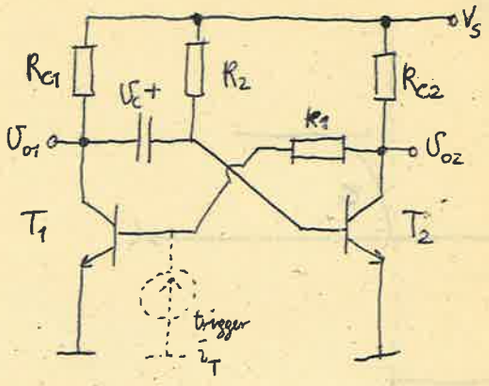
Triggering from collectors :



R	S	D_1	D_2	y_{n+1}
0	1	ON	OFF	0
1	0	OFF	ON	1
1	1	OFF	OFF	y_n
0	0			not used

Pulse Generators

Collector coupled monostable multivibrator



Has 2 states :

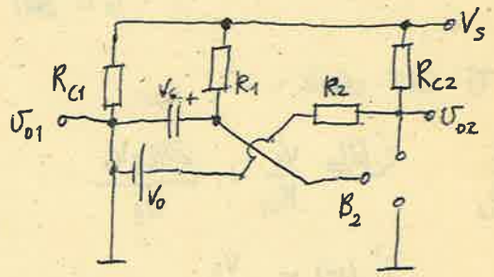
1) Stable state
2) Quasi stable (pulse) state

$t = 0^-$, the circuit is at steady state (i.e stable state)
C open. Assume T_2 SAT ; T_1 OFF

$v_c(0) = V_0 - V_s$

At $t = 0$, trigger is applied.

T_1 SAT , T_2 ~~OFF~~.



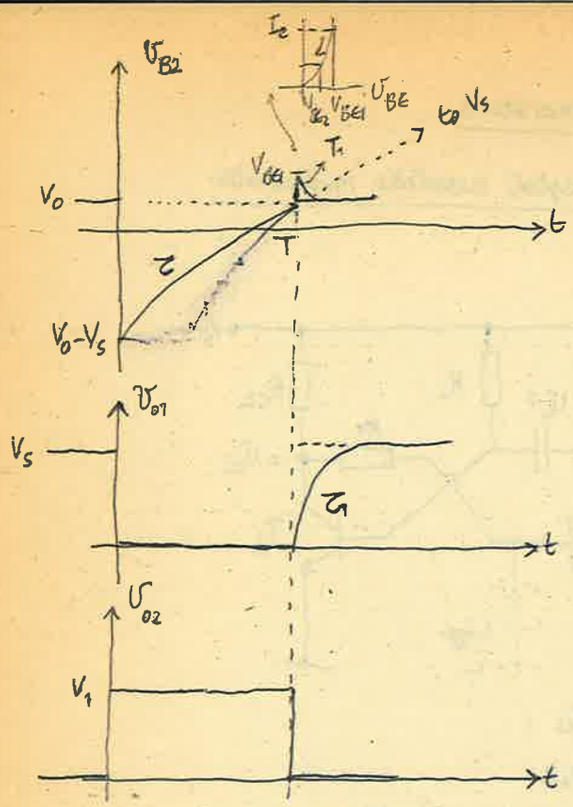
$v_{o1}(t) = 0$

$$v_{o2}(t) = \frac{(V_s - V_0)}{R_{C2} + R_2} R_2 + V_0 \triangleq V_1$$

$v_{B_2}(0^+) = v_c(0) = V_0 - V_s$

$v_{B_2}(\infty) = V_s$

$\tau = R_1 C$



$$v_{B_2}(t) = V_S + [V_0 - 2V_S]\, e^{-t/\tau}$$

$$v_{B_2}(T) = V_S + [V_0 - 2V_S]\, e^{-T/\tau} = V_0$$

$$T \cong \tau \ln 2 \approx 0{,}7\tau$$

$$v_C(T) = v_{B_2}(T^-) = V_0$$

At $t = T$, regenerative switching occurs and T_1 is OFF
T_2 is SAT

$0 < t < T$ T_1 SAT check :

$$i_{b_1} = \frac{V_S - V_0}{R_{C_2} + R_2} \qquad i_{C_2}(0^+) = \frac{V_S}{R_{C_1}} + \frac{2V_S - V_0}{R_1}$$

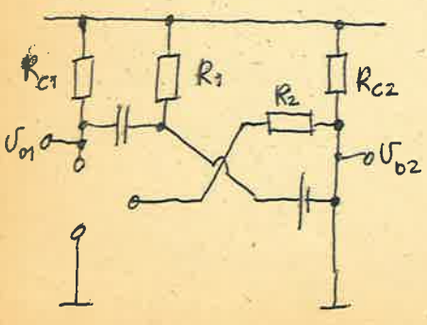
$$i_{C_2}(\infty) = \frac{V_S}{R_{C_1}}$$

$\beta i_{b_1} > i_{C_2 SAT}$

$\beta i_{b_1} > i_{C_2}(0^+)$ must be.

$$\boxed{\beta\left(\frac{V_S - V_0}{R_{C_2} + R_2}\right) > \frac{V_S}{R_{C_1}} + \frac{2V_S - V_0}{R_1}}$$

For $t > T$:



$v_{B_2}(t) = V_0$

$v_{02}(t) = 0$

$v_{01}(T^+) = V_0 - \underbrace{V_C(T)}_{V_0} = 0$

$v_{01}(\infty) = V_S$

$\tau_1 = R_{C_1} C$

Check that T_2 is SAT :

$$i_{C_2} = \frac{V_S}{R_{C_2}}$$

$$i_{b_2}(T^+) = \frac{V_S - V_0}{R_1} + \frac{V_S + 2V_0}{R_{C_1}}$$

$$i_{b_2}(\infty) = \frac{V_S - V_0}{R_1}$$

$\beta i_{b_2} > i_{C_2}$

$\beta i_{b_2}(\infty) > i_{C_2} \Rightarrow T_2$ SAT.

$$\boxed{\beta\,\frac{(V_S - V_0)}{R_1} > \frac{V_S}{R_{C_2}}}$$

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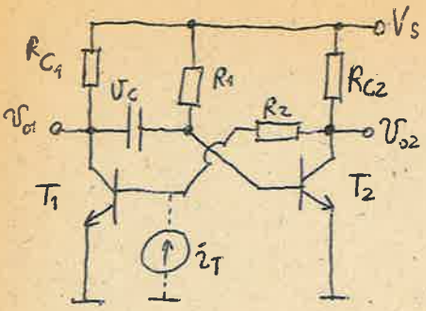
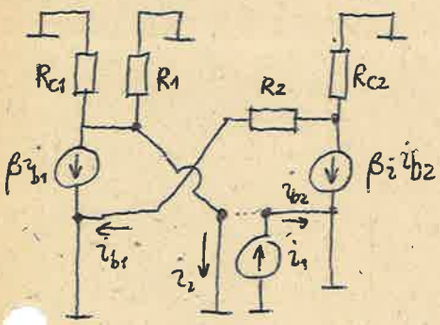


Loop gain calculation:



Since switching takes place in very short time, the voltage on 'C' will not change ∴ it is short ckt.

$$i_2 = -\beta_1 i_{b1} \qquad i_{b1} = -\frac{\beta_2 i_{b2} R_{C2}}{R_2 + R_{C2}} \qquad i_{b2} = i_1$$

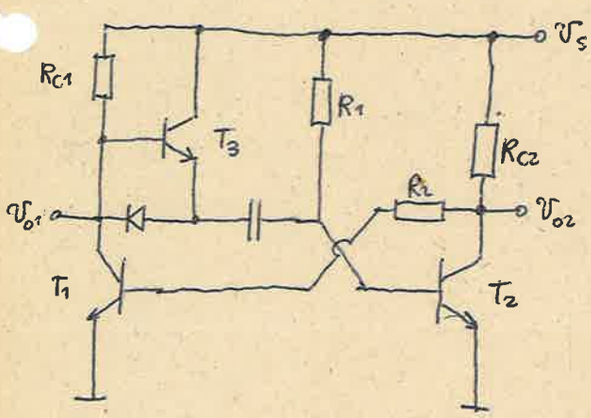
$$i_2 = \frac{\beta_1 \beta_2 R_{C2} i_1}{R_2 + R_{C2}}$$

$$\boxed{A_L = \frac{\beta_1 \beta_2 R_{C2}}{R_2 + R_{C2}} > 1}$$

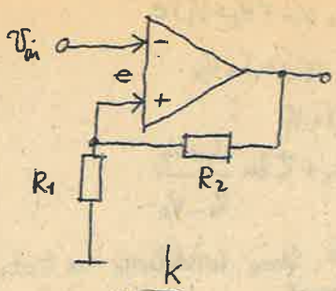
must be satisfied.

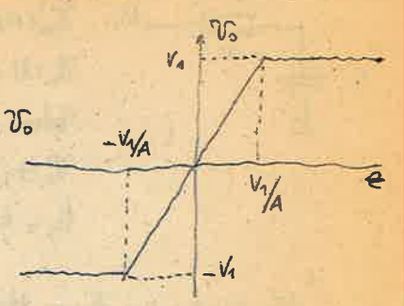
exercise: The SAT conditions of the transistors will also give the above inequality.

To decrease the recovery time of V_{o1}:



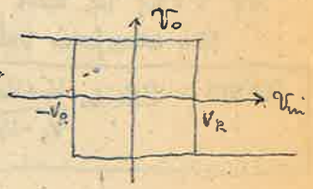
An astable multivibrator using a regenerative comparator

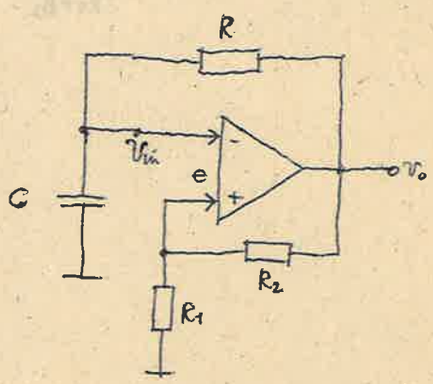




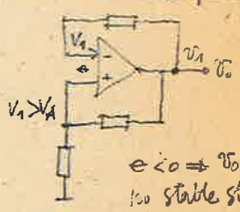
k

$$A_L = \frac{A R_1/(R_1+R_2)}{} = Ak > 1 \Rightarrow$$



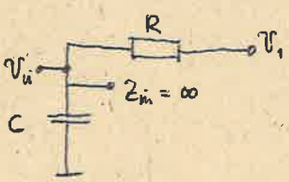


Suppose monostable at S.S ⇒ C open



$e < 0 \Rightarrow V_o \to -V_1$
∴ stable state at S.S.
∴ it is not monostable

Assume at $t=0$, $V_c(0)=0$, $V_o(0)=V_1$



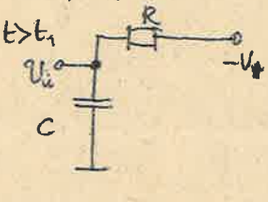
$V_{in}(\infty) = V_1$
$V_{in}(0) = 0$
$\tau = RC$

$$V_{in}(t) = V_1 - V_1 e^{-t/\tau}$$

When $V_{in}(t_1) = V_R \Rightarrow V_o = -V_1$

$$t_1 = \tau \ln \frac{V_1}{V_1 - V_R}$$

For $t > t_1$

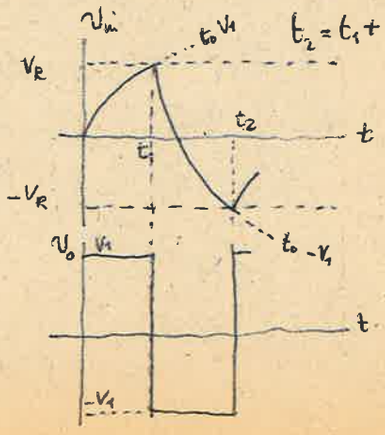


$V_{in}(t_1^+) = V_R$
$V_{in}(\infty) = -V_1$

$$V_{in}(t) = -V_1 + (V_1 + V_R) e^{-(t-t_1)/\tau}$$

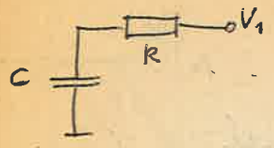
When $V_{in}(t_2) = -V_R \Rightarrow V_o(t_2) = V_1$

$$t_2 = t_1 + \tau \ln \frac{V_1 + V_R}{V_1 - V_R}$$



→

For $t > t_2 \Rightarrow$



$v_{in}(t_2^+) = -V_R$

$v_{in}(\infty) = V_1$

$v_{in}(t) = V_1 - (V_R + V_1)\, e^{-(t-t_2)/\tau}$

When $v_{in}(t_3) = V_R$

$v_o(t_3) = -V_1$

$$t_3 = t_2 + \tau \ln \frac{V_1 + V_R}{V_1 - V_R}$$

At $t = t_3$ we have the same conditions as $t = t_1$

$\therefore$ the waveforms will repeat

$$\text{PERIOD} = 2RC \ln \frac{V_1 + V_R}{V_1 - V_R}$$

$T = t_3 - t_1 = 2(t_2 - t_1)$

$V_R \cong kV_1 \quad k = \frac{R_1}{R_1 + R_2}$

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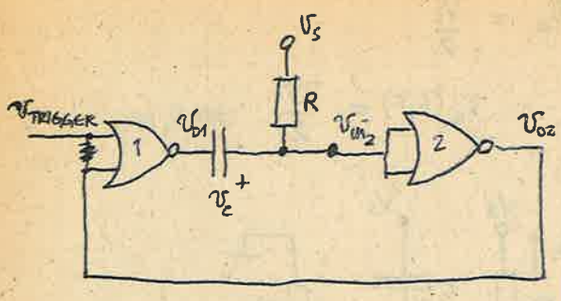
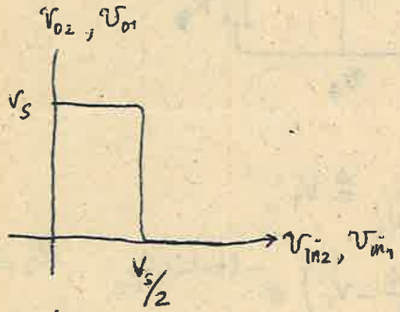
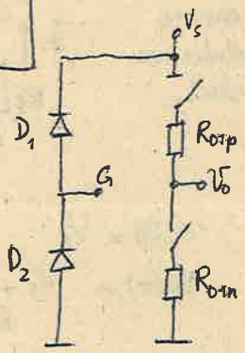
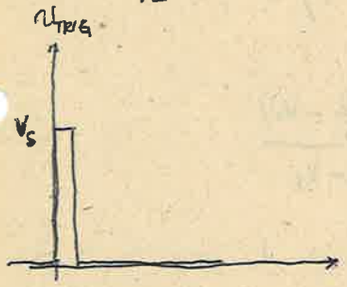
CMOS Monostable Multivibrator









$t = 0^-$: the circuit is at stable state
C is open.

$V_{in_2}(0^-) = V_S$

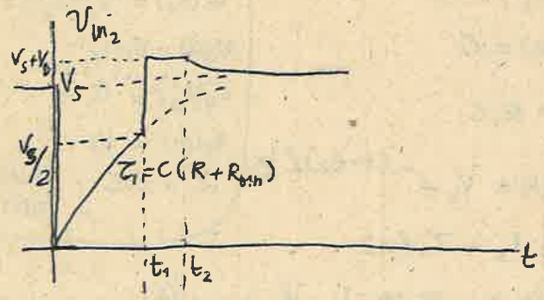
$\therefore V_{o_2}(0^-) = 0$

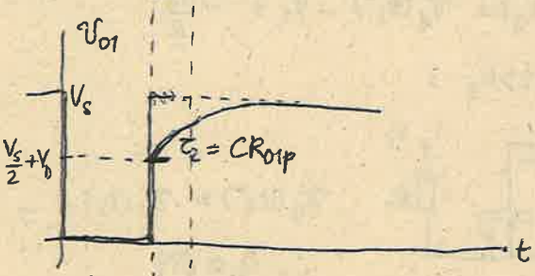
$V_{o_1}(0^-) = V_S$

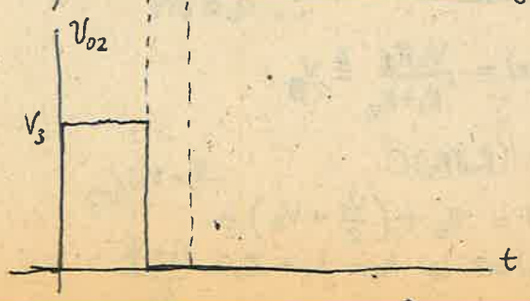
$V_c(0^-) = 0$

$V_{o_1}(0^-) = \overline{V_{TR}(0^-) + V_{o2}(0^-)}$

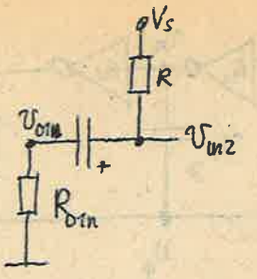
$= V_S$







$t = 0^+$: $V_{o_1}(0^+) = 0$ (due to trigger)



Assume the voltage drop across R_{o1n} is negligible.

$V_{in_2}(0^+) \cong 0\ (V_c(0)) \Rightarrow V_{o_2}(0^+) = V_S$

$V_{in_2}(t) = V_S - V_S e^{-t/\tau_1}$

$V_{in_2}(t_1) = V_S - V_S e^{-t_1/\tau_1}$

$t_1 = \tau_1 \ln 2 = 0.7\tau_1$

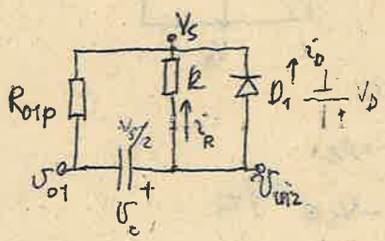
$V_c(t_1) = V_{in_2}(t_1^-) = \frac{V_S}{2}$

For $t > t_1$

At $t = t_1^+$ V_{o1} is H $\Rightarrow V_{in_2}(t_1^+) = V_c(t_1^+) + V_{o1}(t_1^+)$

$> V_S$

$\therefore$ protection diode D_1 of gate 2 is ON.



$V_{in_2}(t_1^+) = V_S + V_D$

$V_{o1}(t_1^+) = V_{in_2}(t_1^+) - V_c(t_1)$

$= \frac{V_S}{2} + V_D$

$V_{o1}(\infty) = V_S$

$V_{in_2}(t) = V_S + V_D$

$i_R = \frac{V_D}{R}$

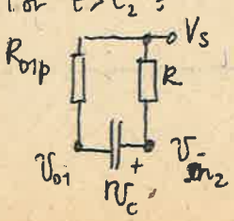
$i_c(t) = i_R + i_D$

At steady state $i_c = 0$ $\therefore$ for some time $t = t_2$,

$i_c(t_2) = i_R$

$\Rightarrow$ at $t = t_2$ D_1 will be OFF

For $t > t_2$:

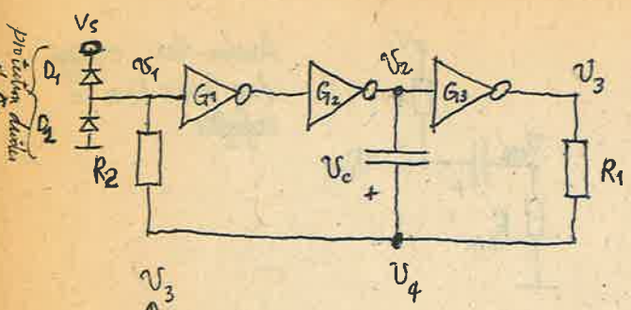


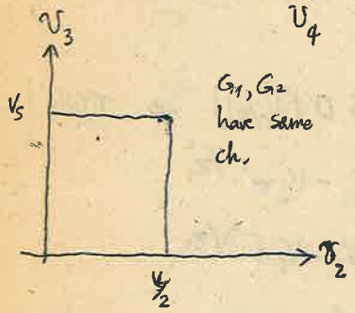
$V_{o1}(\infty) = V_S$

$V_{in_2}(\infty) = V_S$

$\tau_3 = C(R_{o1p} + R)$

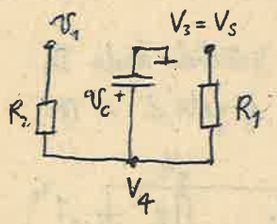
CMOS V astable multivibrator





Assume $v_c(0) = 0$ and $v_1(0) < \frac{V_s}{2} \Rightarrow v_2(0) = 0$, $v_3(0) = V_s$

~~$v_3 = V_s$~~



$v_4(0) = v_c(0) = 0$

$v_4(t) = v_1(t)$

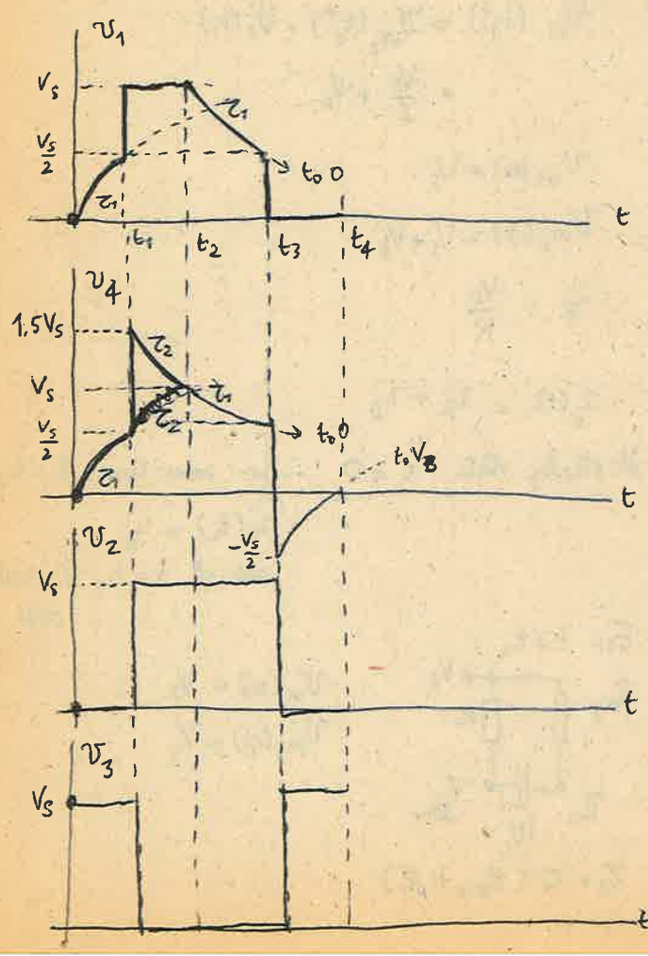
so $v_1(0) = 0$

$v_1(\infty) = V_s \quad \tau_1 = R_1 C$

$v_1(t) = V_s - V_s e^{-t/\tau_1}$

$v_1(t_1) = \frac{V_s}{2} = V_s - V_s e^{-t_1/\tau_1}$

$t_1 = \tau_1 \ln 2 \cong 0.7\tau_1$



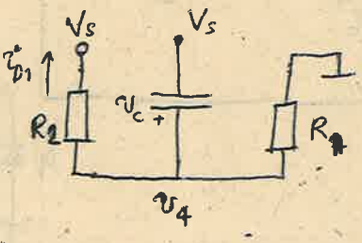
At $t = t_1^+$, $v_2(t_1^+) = V_s$

$v_3(t_1^+) = 0$

$v_c(t_1) = v_4 = \frac{V_s}{2}$

For $t > t_1$ $\quad v_4(t_1^+) = \frac{3V_s}{2} \Rightarrow D_1$ ON.

assume diodes are ideal.



$v_4(t) = V_s$

$v_4(\infty) = V_s \frac{R_1}{R_1 + R_2} \triangleq V_1$

$v_4(t) = V_1 - \left(\frac{3V_s}{2} - V_1\right) e^{-(t-t_1)/\tau_2}$ $\quad \tau_2 = (R_1 // R_2)C$

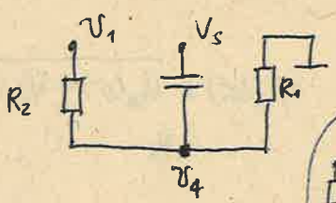
$v_4(t_2) = V_s$

$t_2 = t_1 + \tau_2 \ln \frac{\left(\frac{3V_s}{2} - V_1\right)}{V_s - V_1}$

$i_{D1}(t_2) = 0$

$\therefore D_1$ OFF

$v_c(t_2) = 0$



$v_4(t) = v_1(t)$

$v_4(t_2^+) = V_s$

$v_4(\infty) = 0$

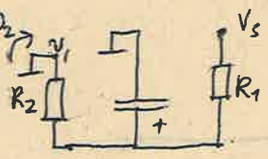
$\tau_1 = R_1 C$

$v_4(t) = V_s e^{-(t-t_2)/\tau_1}$

$t_3 = t_2 + \tau_1 \ln 2$

$v_c(t_3) = v_4(t_3^-) - V_s = -\frac{V_s}{2}$

for $t > t_3$:



$v_4(t_3^+) = v_c(t_3) = -\frac{V_s}{2}$

$\therefore D_2$ is ON

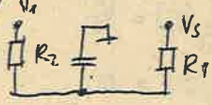
$v_4(\infty) = \frac{V_s R_2}{R_1 + R_2} \triangleq V_B$

$\tau_2 = (R_1 // R_2)C$

$v_4(t) = v_B + \left(\frac{V_s}{2} + V_B\right) e^{-(t-t_3)/\tau_2}$

$v_4(t_4) = 0 \Rightarrow t_4 = t_3 + \tau_2 \ln \frac{V_B + \frac{V_s}{2}}{V_B}$

For $t > t_4$ D_2 OFF:



$v_c(t_4) = v_4(t_4^-) = 0$

$v_4(t) = v_1(t)$

$v_4(t_4^+) = 0$

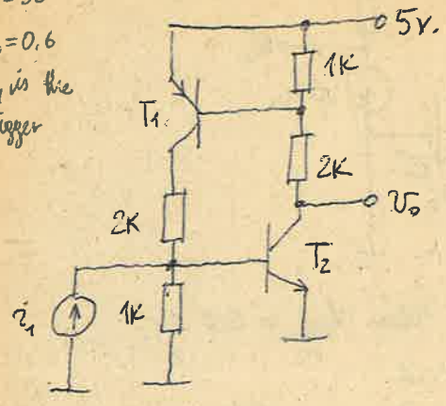
$v_4(\infty) = V_s$

$\tau = R_1 C$ STARTING POINT.

280582

Q12 (Last distributed exercises)

$\beta = 30$
$V_\gamma = 0.6$
i_1 is the trigger

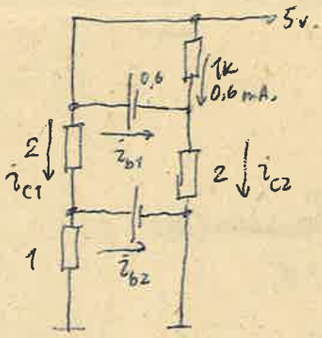


a) the stable states are = ?

1. T_1 SAT, T_2 SAT
2. T_1 OFF, T_2 OFF

b) loop gain ?

d) T_1 SAT, T_2 SAT ? ($i_1 = 0$)



$i_{c1} = \frac{5-0.6}{2} = 2.2$ mA.

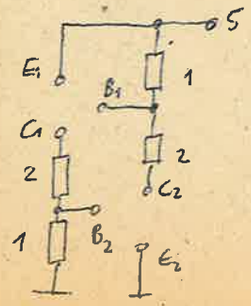
$i_{c2} = \frac{5-0.6}{2} = 2.2$ mA.

$i_{b1} = i_{c2} - 0.6 = 1.6$ mA.

$i_{b2} = i_{c1} - 0.6 = 1.6$ mA.

$\left.\begin{array}{l} \beta i_{b1} > i_{c1} \\ \beta i_{b2} > i_{c2} \end{array}\right\}$ TR's are SAT.

T_1 OFF, T_2 OFF :

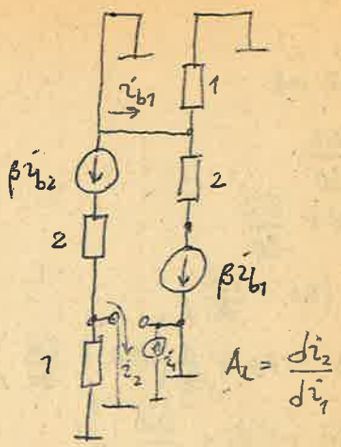


$V_{EB_1} = 0 < 0.6$

$V_{CB_1} = -5 < 0.6$

$\therefore$ T_1 OFF, T_2 OFF

b)



$i_1 = i_{b2}$

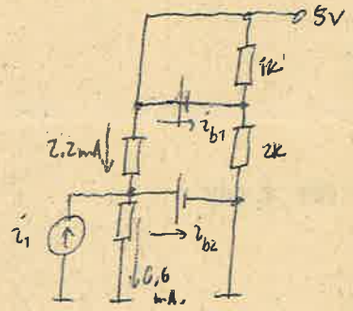
$i_{b1} = \beta i_{b2}$

$i_2 = \beta i_{b2} = \beta^2 i_1$

$A_L = \beta^2 = 900$

c) T_1 SAT, T_2 SAT $\longrightarrow$ T_1 OFF, T_2 OFF

$i_1 = ?$



Find i_1 for which both transistors are active.

$i_{c2} = 2.2$ mA. independent of i_1

$i_{b1} = 1.6$ mA " " "

$i_{c1} = 2.2$ mA " " "

$i_{b2} = i_1 + 1.6$ mA.

When T_2 is just ACT, $V_{CE_2} = 0$ V.

$\therefore$ $i_{c2} = 2.2$ mA.

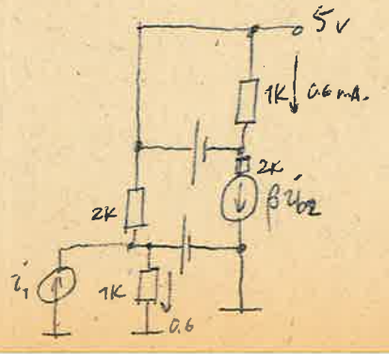
$i_{b1} = 1.6$ mA.

$i_{c1} = 2.2$ mA.

$\beta i_{b1} > i_{c1} \Rightarrow T_1$ remains SAT.

$i_{b2} = \frac{2.2}{30}$

$i_1 = -2.2 + 0.6 + \frac{2.2}{30} = -1.53$



When T_1 is just ACT :

$v_{CE1} = 0$

$\therefore i_{C1} = 2.2$ mA.

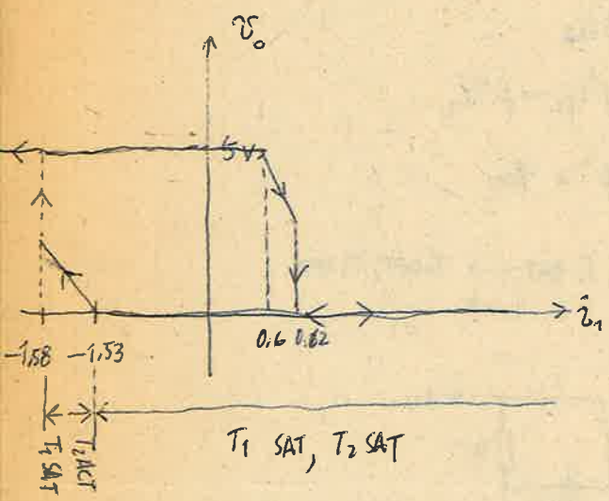
$i'_{b1} = \frac{2.2}{30}$

$\beta i'_{b2} = 0.6 + \frac{2.2}{30}$

$i'_{b2} = \frac{1}{30}\left(0.6 + \frac{2.2}{30}\right)$

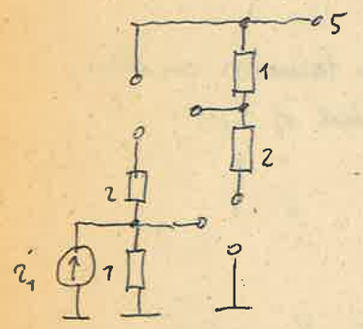
$i'_1 = -2.2 + 0.6 + \frac{1}{30}\left(0.6 + \frac{2.2}{30}\right)$

$$i'_1 = -1.6 + 0.02 + \frac{2.2}{900}$$

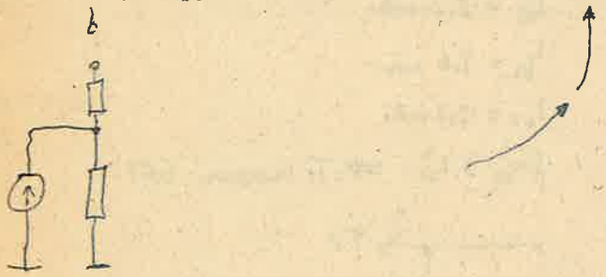


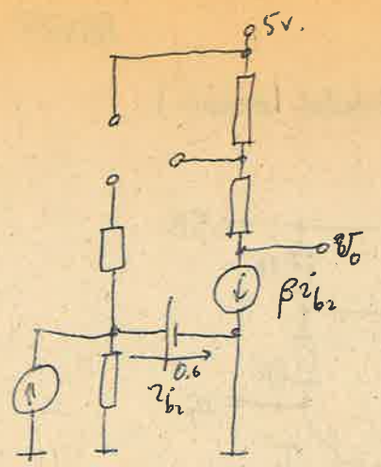
d) T_1 OFF, T_2 OFF ⟶ T_1 SAT, T_2 SAT

$i_1 = ?$



$i'_1 = 0.6$ mA ⇒ $V_{BE} = 0.6$ T_2 becomes ACT.





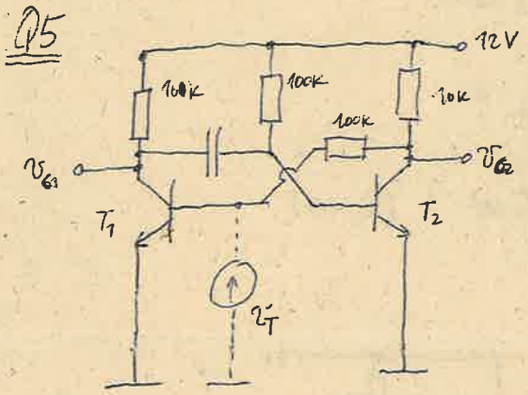
T_1 becomes ACT when $V_{EB_1} = 0.6$ V.

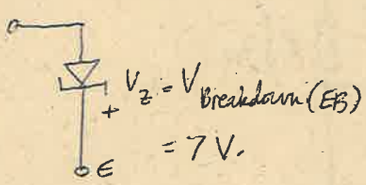
$\therefore \beta i_{b2} = 0.6$ mA.

it means that $i_{b2} = \frac{0.6}{30}$

$i'_1 = 0.6 + \frac{0.6}{30} = 0.62$ mA.

Q5





Find v_{C1}, V_{C2}, V_{B2}

$t = 0^-$ s.s. C open.

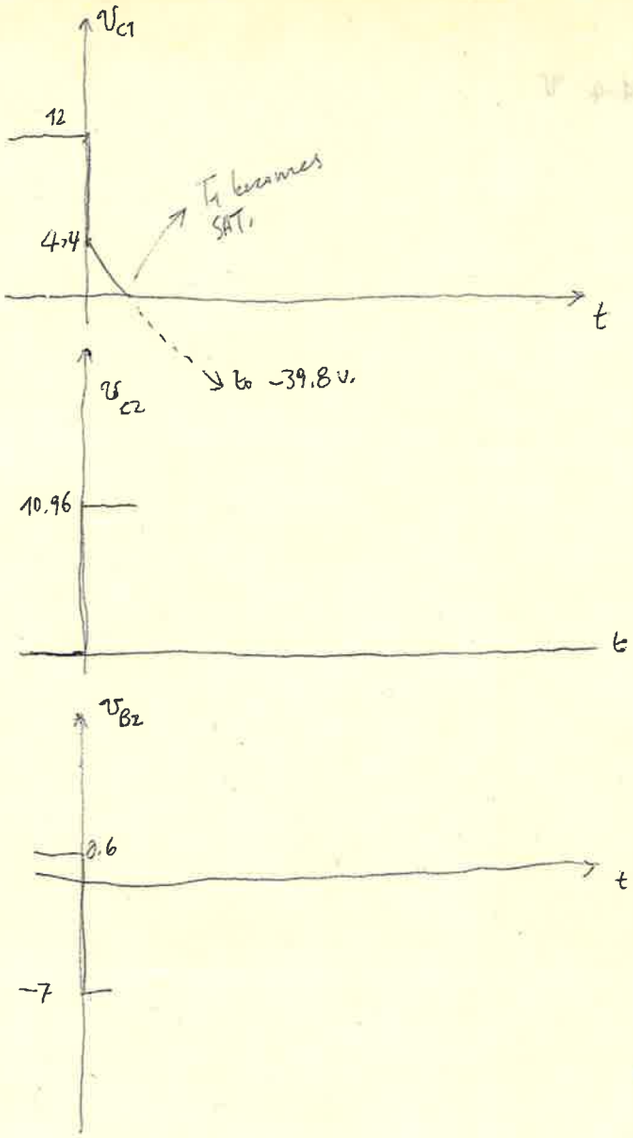
Assume T_2 SAT, T_1 OFF

$i_{b2} = \frac{12 - 0.6}{100}$ $\quad i_{c2SAT} = \frac{12}{10} = 1.2$mA.

$\beta i_{b2} > i_{c2SAT}$; T_2 SAT.

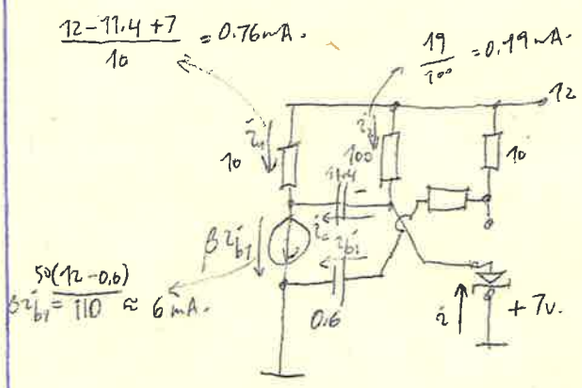
So T_1 OFF $(V_{BE_1} = 0)$

$v_C(0) = -11.4$ V.



At $t=0^+$ if T_1 is SAT, then $v_{B2}(0^+) = -11.4$ v. This forces the Zener to be ON and hence we have inconsistency.

$\therefore$ T_1 has to be ACT.



$i_c = \beta i_{b1} - i_1 = 6 - 0.76 = 5.24$

$i_{b2} \cong 0.12$mA. Assume Zener ON. $i_z(0^+) = i_c - i_2 = 5.24 - 0.19 > 0$ ✓ Z ON.

$v_{C2} = \frac{12-0.6}{110} \times 100 + 0.6 \triangleq V_A = 10.96$ V,

$v_{c1}(0+) = -V_z - V_c(0) = -7 + 11.4 = 4.4\ v.$

$v_{B2} = -V_z = -7\ v.$

$v_{c1}(\infty) = 12 - 10K\beta\frac{12-0.6}{110}$

$= -39.8\ v,$

$\tau = 10K * 10\,nF = 100\,\mu sec.$

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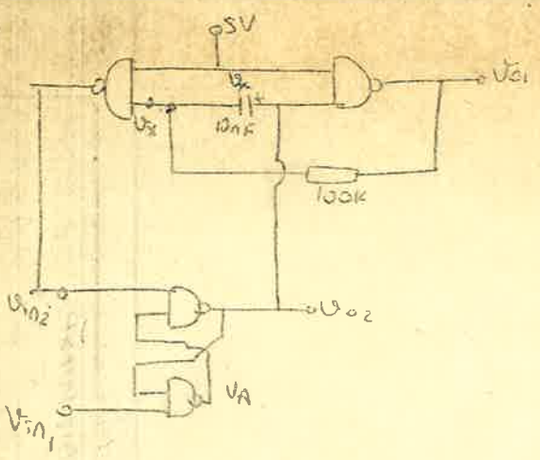
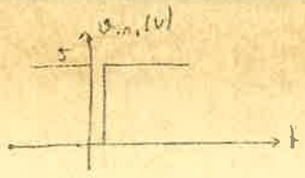
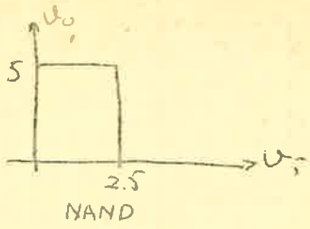
Q7/







At $t=0^-$ circuit is at steady state ; i.e. Open

Find the steady state values v_{o1} and v_{o2}

Assume $v_{o2}(0^-) = 0$. Check

$v_{o1}(0^-) = \overline{v_{o2}(0^-).5V} = 5V$

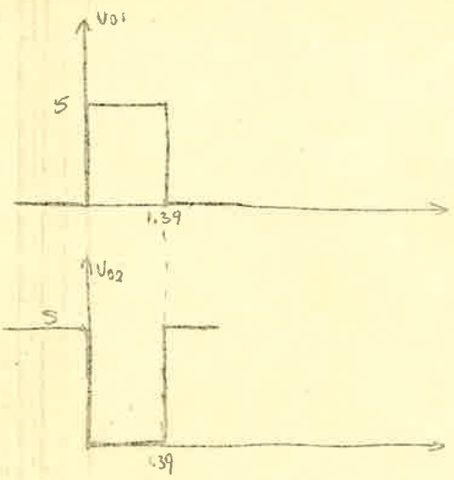
$v_x(0^-) = v_{o1}(0^-) = 5V$ $\quad\therefore\ v_{in_2}(0^-) = 5 \times v_x(0^-) = 0V.$

$\therefore\ v_{o2}(0^-) = 5V$ $\quad\Rightarrow$ $v_{o2}(0^-)=0$ is not steady state solution (stable)

$\therefore$ assume $v_{o2}(0^-) = 5V$

$v_{o2}(0^-) = 5v$ comes out to be the steady state solution.

$v_{o1}(0^-) = \overline{5 . v_{o2}(0^-)} = 0$



At $t=0^+$, $v_{in_1}(0^+)=0$

$v_A(0^+)=5V$

$v_c(0) = v_{o2}(0^-) - v_x(0^-) = 5V$

Assume $v_{o2}(0^+) = 5v$

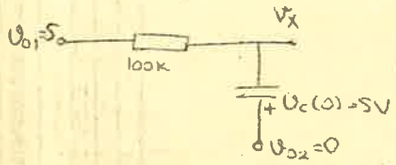
$v_x(0^+) = v_{o2}(0^+) - v_c(0) = 0v$

$\therefore\ v_{in_2}(0^+) = 5v$

$\therefore\ v_{o2}(0^+) = 0v$ ✓

$v_{o1}(0^+) = \overline{v_{o2}(0^+).5} = 5v$

Equivalent circuit.



$v_x(0^+) = -v_c(0) = -5v$

$v_x(\infty) = 5v$

$\tau = 1ms$

$v_x(t) = 5 - 10\, e^{-t/1}$ $\quad t, ms$

$v_x(t_1) = 2.5 = 5 - 10\, e^{-t_1/1}$ $\Rightarrow t_1 = \ln \frac{10}{2.5} = 1.39$

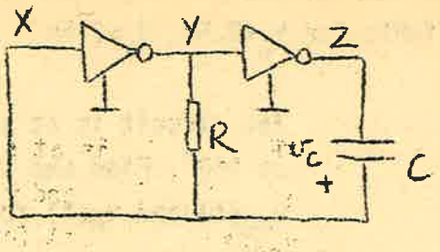
For $t = t_1^+$, $v_{in_2}(t_1^+) = 0$

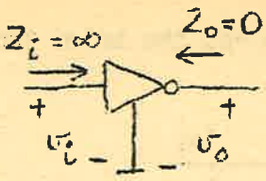
$\therefore\ v_{o2}(t_1^+) = 5V$ and $v_{o1}(t_1^+) = 0v$.

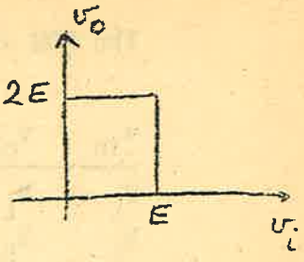
$\therefore$ mono stable

EE 411
Exercise

Q.1.

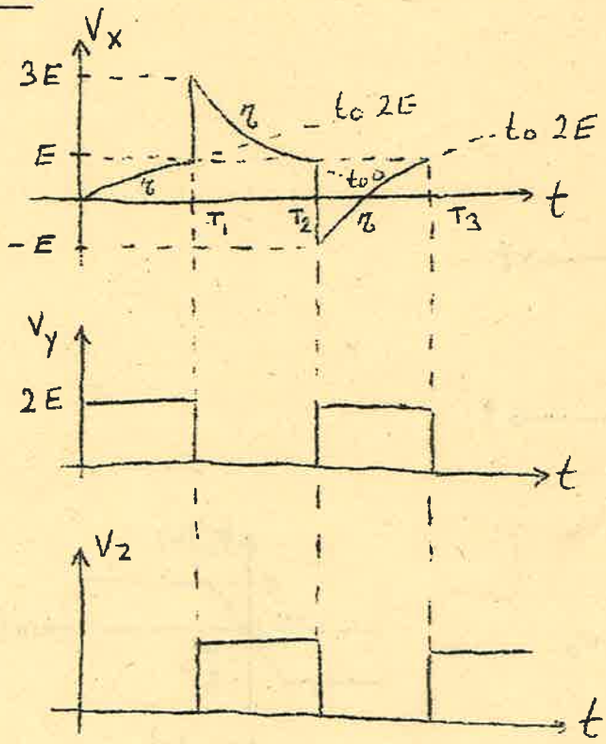






The inverters used in the above circuit have the characteristic shown. Assuming the initial conditions $v_y(0) = 0$ and $v_x(0) = 0$ calculate and plot a few cycles of $V_x(t)$, $V_y(t)$ and $V_z(t)$ interms of R,C and E for the square wave generator shown. Find and expression for the frequency.

ANS:



$\tau = RC$

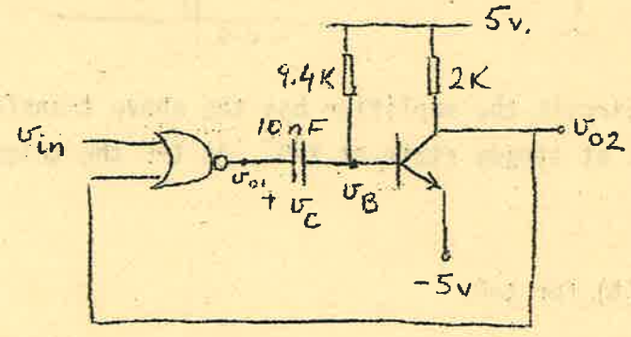
$T_1 = RC \ln 2$

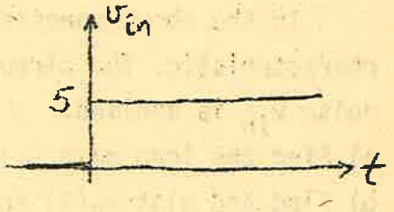
$T_2 - T_1 = RC \ln 3$

$T_3 - T_2 = RC \ln 3$

$$f = \frac{1}{2RC \ln 3}$$

Q.2.





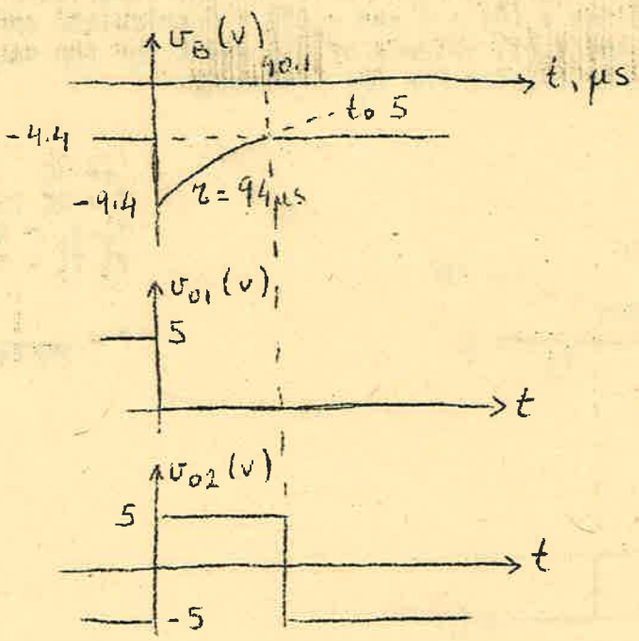
$V_o = 0.6v$, $\beta = 20$

The NOR gate has the below truth table for V_L<2.5v, V_H>2.5v.

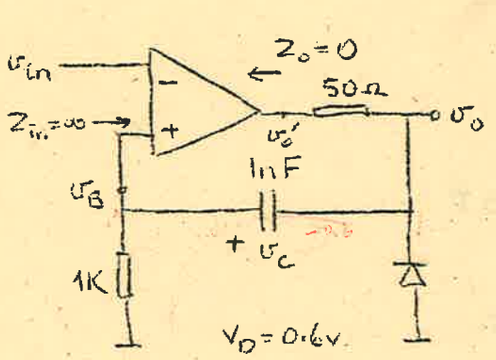
v_{in}	v_{02}	v_{01}
V_L	V_L	5v.
V_L	V_H	0v.
V_H	V_L	0v.
V_H	V_H	0v.

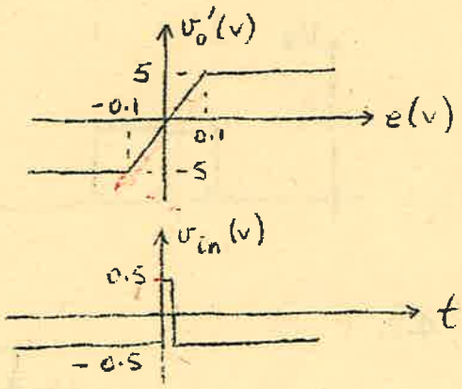
The circuit is at steady state at $t=0^-$. Find and plot $v_{01}(t)$, $v_{02}(t)$ and $v_B(t)$ for t>0.

ANS:



0.3.



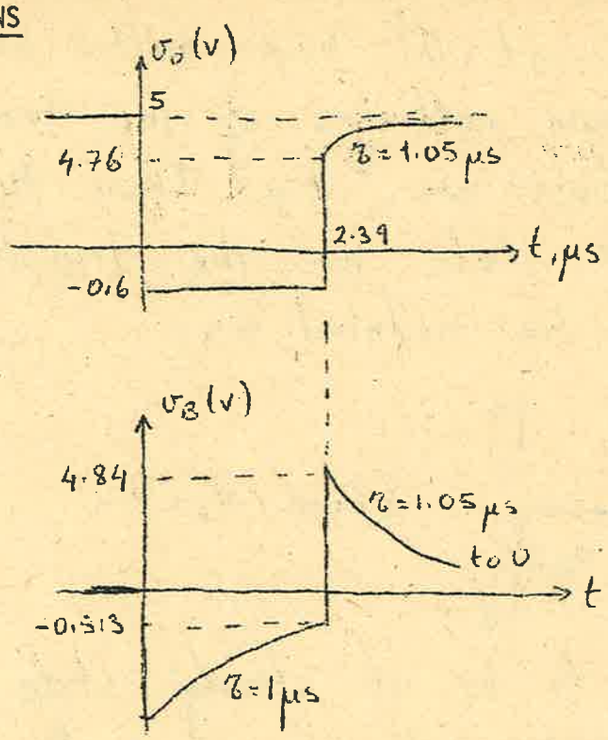


In the above monostable circuit the amplifier has the above transfer characteristic. The circuit is at steady state at $t=0^-$. At t=0 the triggering pulse v_{in} is applied.

a) Find the loop gain

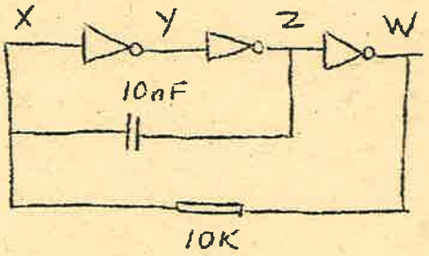
b) Find and plot $v_B(t)$ and $v_o(t)$ for t>0.

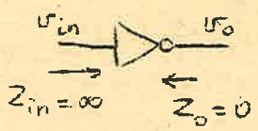
ANS

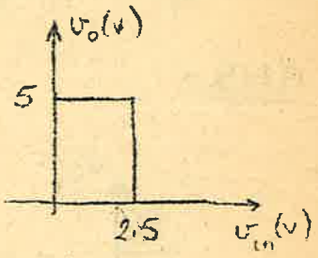


$$A_L = \frac{50}{1050} \times 1000$$

✓ 0.4.

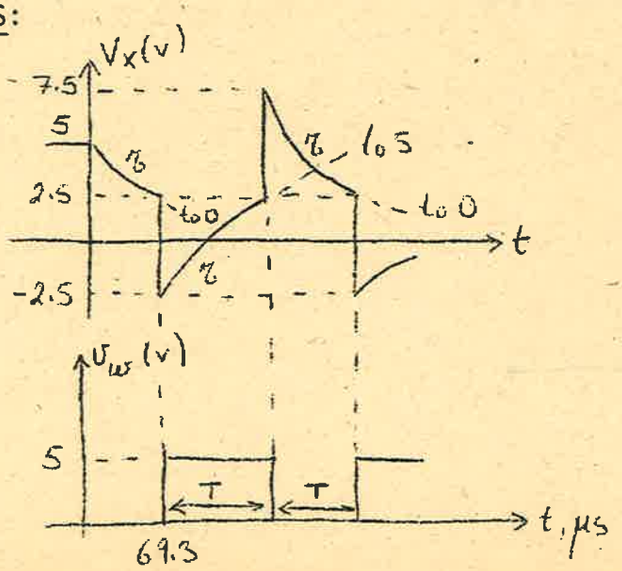






In the above astable circuit assume $v_x(0)=5v$. Find and plot a few cycles of $v_x(t)$, $v_w(t)$ for $t \geq 0$. What is the frequency?

ANS:

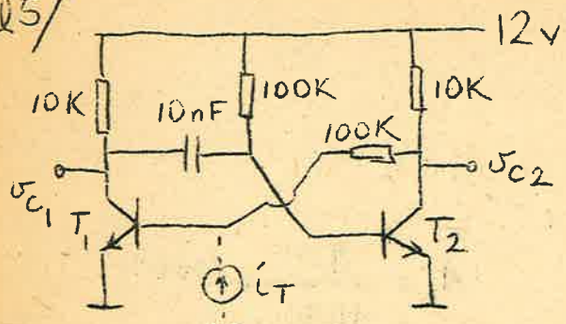


$T = 109.86$ s

$\tau = 100\mu s$

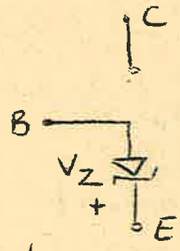
$$f = \frac{10^6}{200 \ln 3} \text{ Hz}$$

Q5/



$\beta = 50$, $V_\gamma = 0.6V$

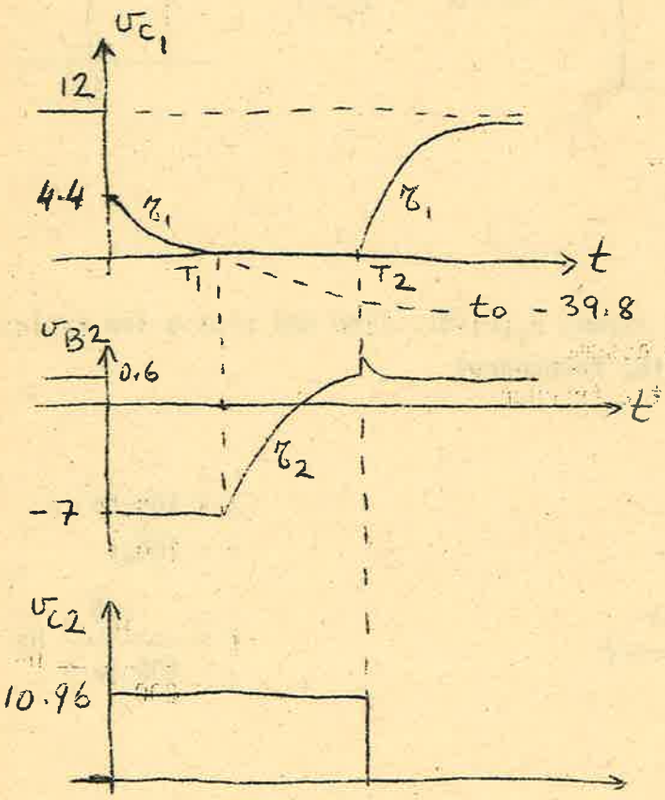
In the given monostable circuit the base-emitter break-down voltages of the transistors are -7 v. Then the OFF state for the transistors can be modeled as:



where $V_Z = 7$ v.

The circuit is assumed to be at steady state at $t = 0^-$. At $t = 0$ a narrow trigger pulse i_T is applied. Plot $v_{C_1}(t)$, $v_{B_2}(t)$ and $v_{C_2}(t)$ for $t \geq 0$.

ANS:



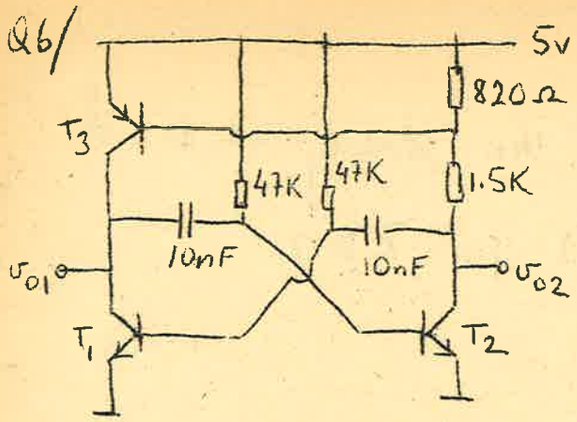
$\tau_1 = 100\mu s$

$\tau_2 = 1ms$

$T_1 = 10.5\mu s$

$T_2 = 520.5\mu s$.

Q6/

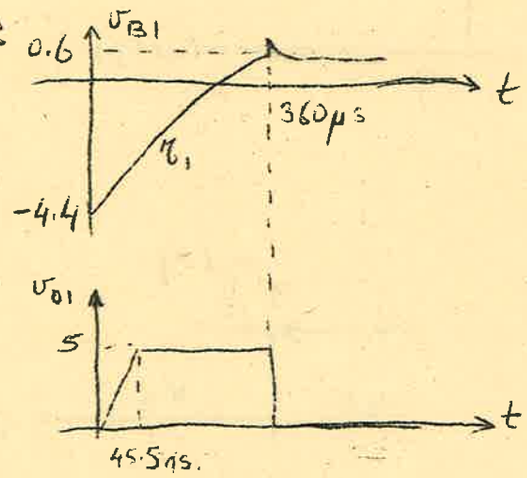


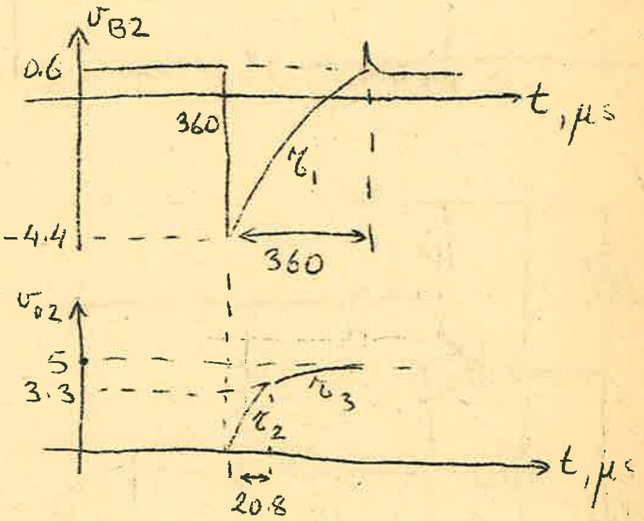
Calculate and plot $v_{o1}, v_{B_1}, v_{o2}, v_{B2}$ for one cycle. What is the improvement gained as compared to the conventional astable?

Hint: Assume that T_1 and T_2 operate between OFF and SAT.

$\beta = 50$, $V_o = 0.6v$

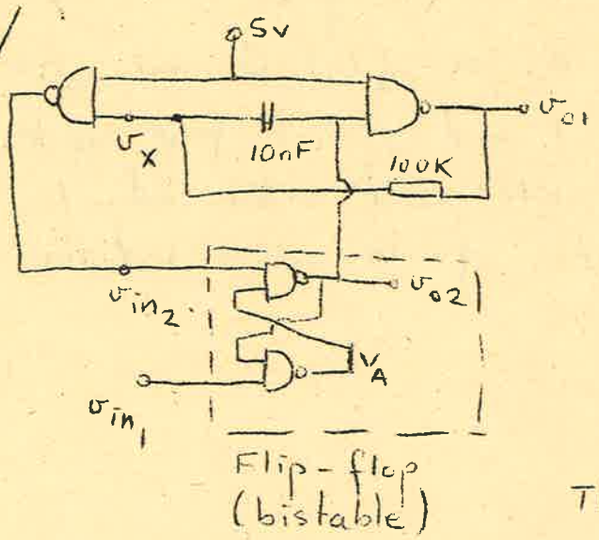
ANS:

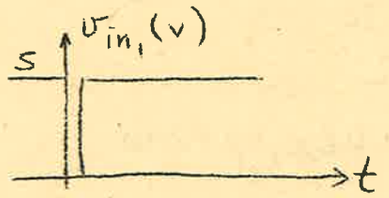




$\tau_1 = 470\,\mu s$, $\tau_2 = 15\,\mu s$, $\tau_3 = 23.2\,\mu s$.

Q7/

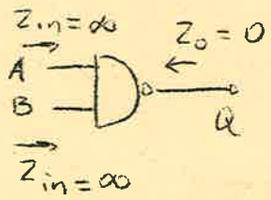


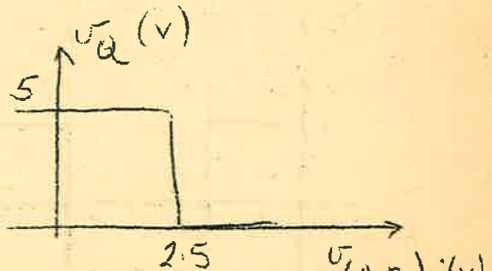


In the given circuit v_{in_1} is the triggering pulse. The circuit is at steady state at $t = 0^-$.

The truth table of the flip-flop and the characteristics of the NAND gates are given below:

v_{in_1}	v_{in_2}	$v_{o2\,n+1}$
0	1	0
1	0	1
1	1	$v_{o2\,n}$
0	0	1

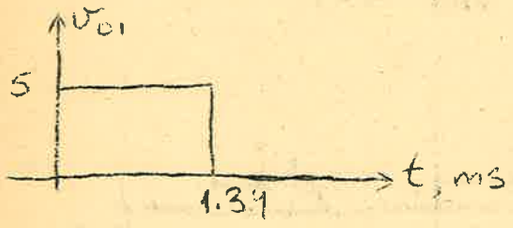


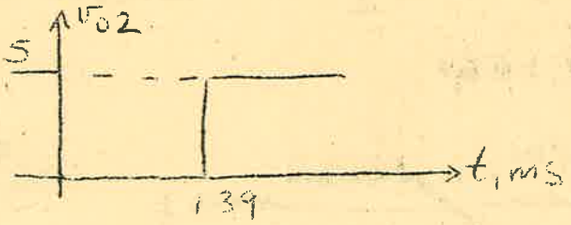


a) Show that $v_{o2}(0^-) = 0$ can not be the steady state solution ⑥

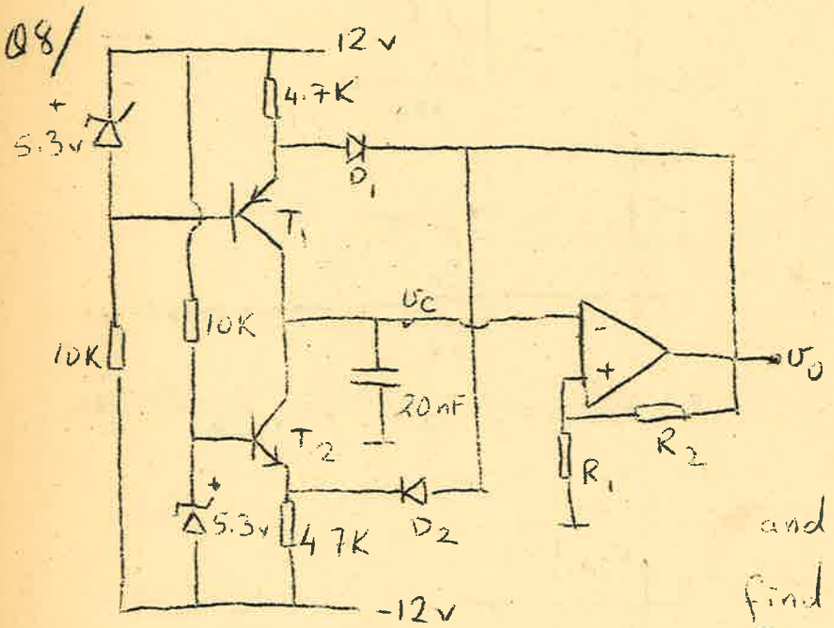
b) Find and plot $v_{o1}(t)$ and $v_{o2}(t)$ for $t \geq 0$.

ANS:

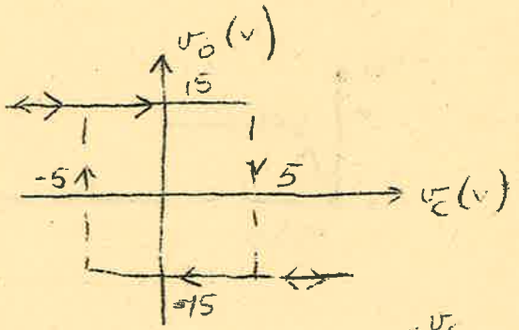




Q8/

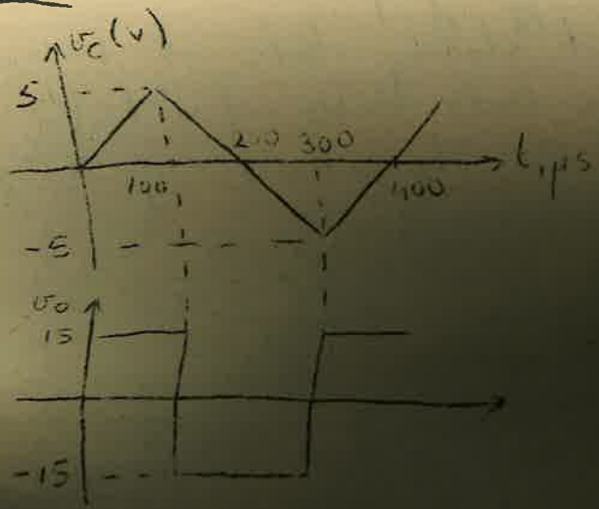


$V_\gamma = 0.6v$, $V_D = 0.6v$, $\beta = 200$

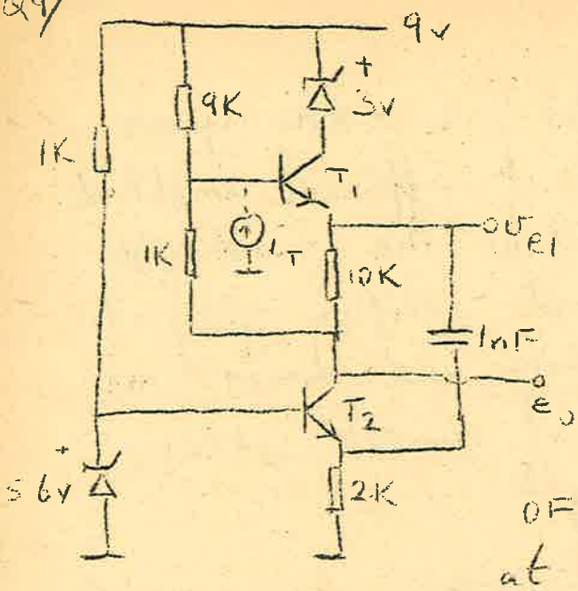


For the given v_o vs. v_c and for $v_c(0) = 0$ and $v_o(0) = 15v$ find and plot a few cycles of $v_c(t)$ and $v_o(t)$ indicating the states of the TRs and the diodes. What is the frequency?

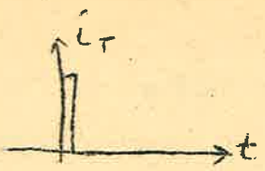
ANS:



Q9/

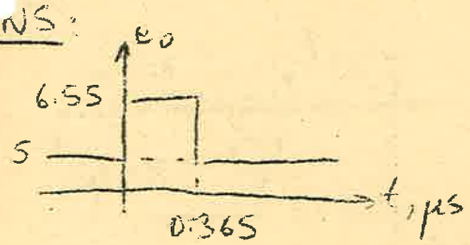


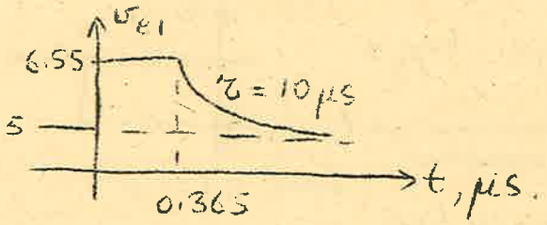
$V_\gamma = 0.6v$, $\beta = 50$



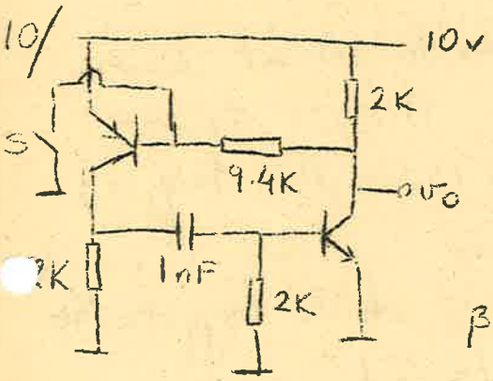
The given monostable circuit is at steady state at $t=0^-$. Using the transistor state finding algorithm show that, at steady state, T_1 is OFF, T_2 is SAT. When i_T is applied at $t=0$, T_1 is forced into SAT. Find and plot $e_o(t)$ and $v_{e1}(t)$ for $t \geq 0$.

ANS:





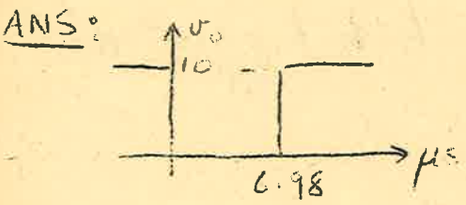
Q10/



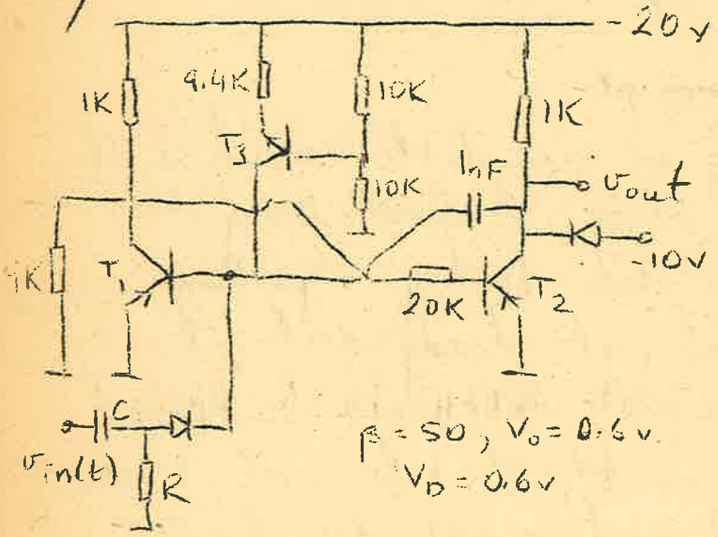
The monostable circuit is at steady state at $t=0^-$. At $t=0$, S is momentarily closed and opened. Find and plot $v_o(t)$ for $t \geq 0$.

$\beta = 20$, $V_\gamma = 0.6v$

ANS:



Q11/

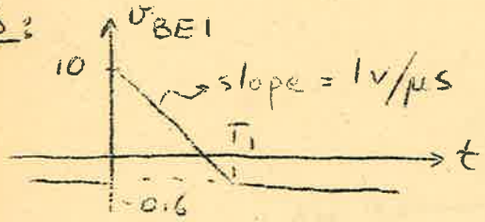


$\beta = 50$, $V_\gamma = 0.6v$
$V_D = 0.6v$

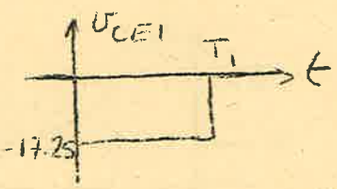
$v_{in}(t)$ is a 50 KHz square wave of sufficient amplitude to trigger the monostable at each positive going edge. Calculate and draw one cycle of $v_{CE_1}(t)$, $v_{out}(t)$, $v_{BE_1}(t)$.

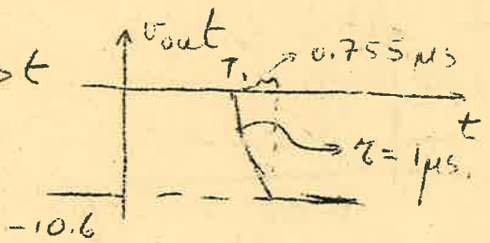
Hint: T_3 serves as a current source.

ANS:

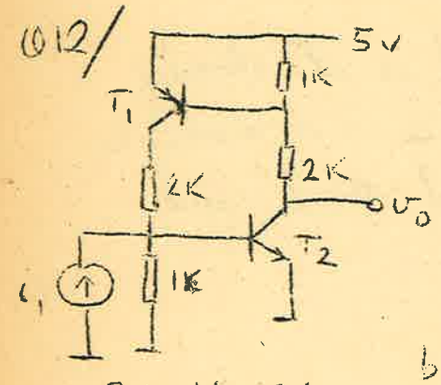


$T_1 = 10.6\mu s$.





Q12/



$\beta = 30$, $V_\gamma = 0.6v$

a) For the given bistable circuit show that 1) T_1 SAT, T_2 SAT 2) T_1 OFF, T_2 OFF are the stable states. (i_1 is the trigger)

b) Find the loop gain

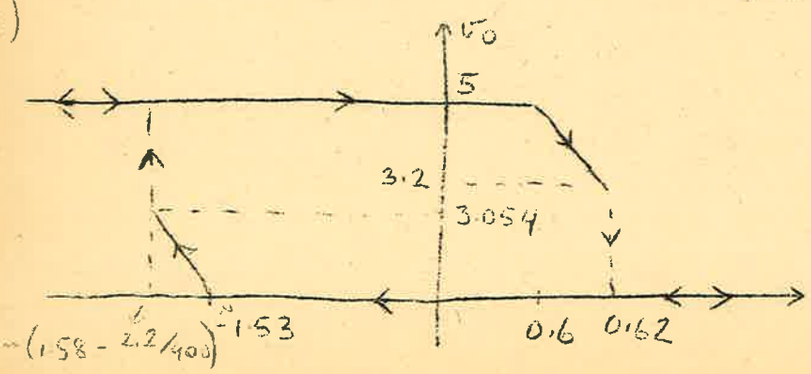
c) Find the value of i_1 which triggers the bistable from state (1) to (2).

d) Find the value of i_1 which triggers the bistable from state (2) to (1).

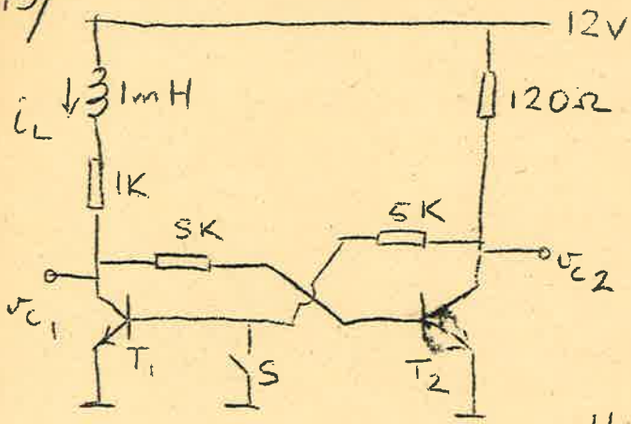
e) Calculate and sketch v_o vs. i_1.

ANS: b) $A_L = 900$ c) $i_1 = -\left(1.58 - \frac{2.2}{900}\right)mA$ d) $i_1 = 0.62\,mA$

e)



Q13/

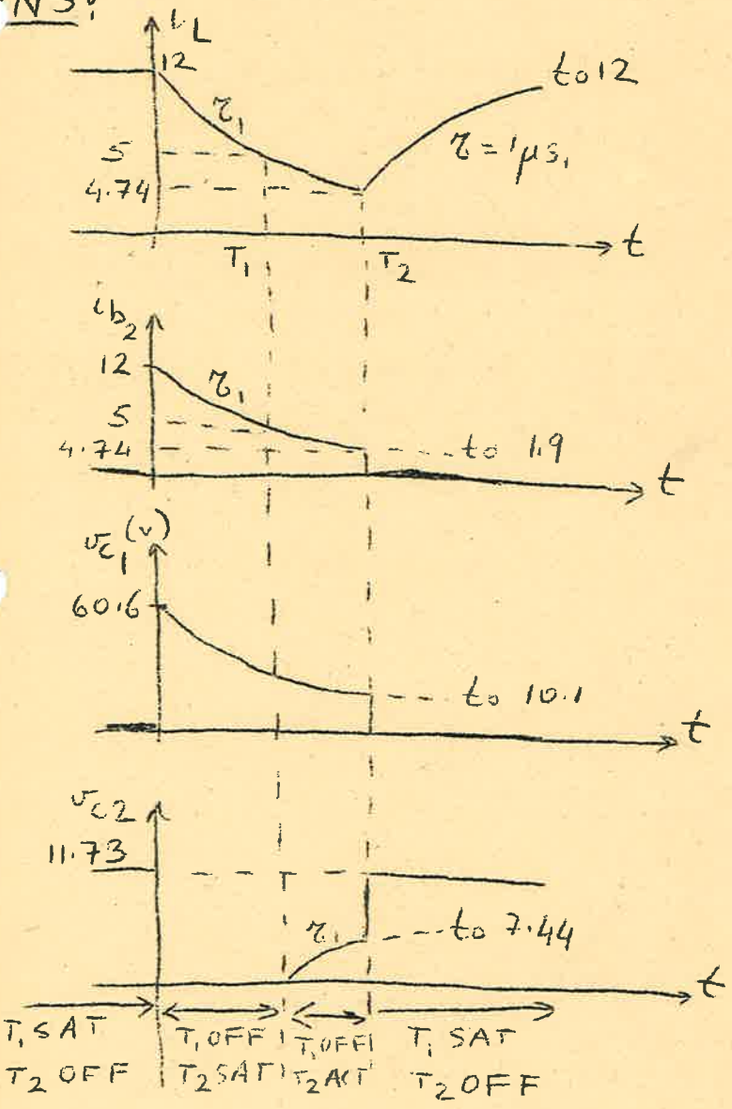


$\beta = 20$, $V_\gamma = 0.6V$

In the given monostable S is open. At $t=0$ it is momentarily closed and opened to trigger the circuit. Determine and plot v_{c1}, v_{c2}, i_{b2}, i_L. Find the loop gain.

Hint: At steady state T_1 is SAT, T_2 is OFF

ANS:



$A_L = 9.375$

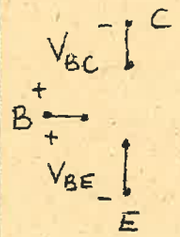
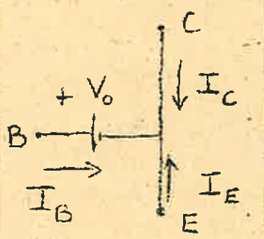
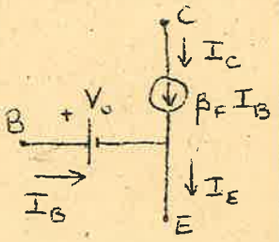
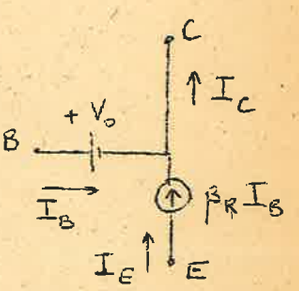
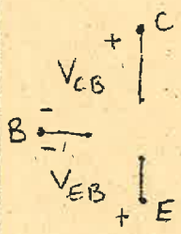
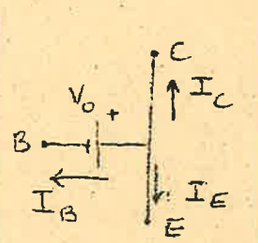
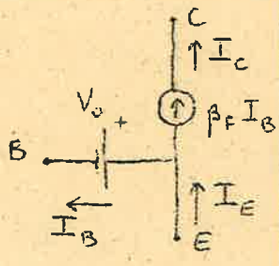
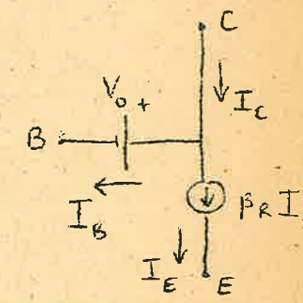
$T_1 = 0.197\mu s$

$T_2 = 0.211\mu s$

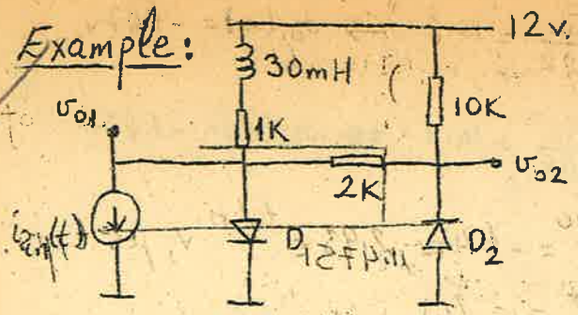
$\tau_1 = \frac{1}{6}\mu s$.

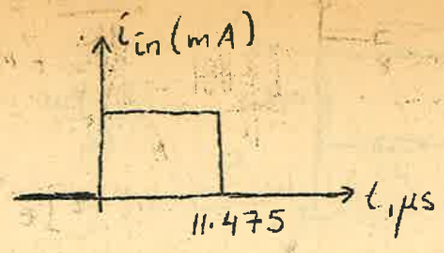
EE 411

TABLE OF SIMPLIFIED COMMON – EMITTER TRANSISTOR MODELS –

	CUTOFF		SATURATION		ACTIVE		REVERSE ACT	
	D(BE) OFF	D(BC) OFF	D(BE) ON	D(BC) ON	D(BE) ON	D(BC) OFF	D(BE) OFF	D(BC) ON
NPN Conditions for validity	$V_{BE} < V_o$ $V_{BC} < V_o$		$\beta_F I_B > I_C$ or $\beta_R I_B > I_E$		$V_{BC} < V_o$ $I_B > 0$ $(I_C > 0, I_E > 0)$		$V_{BE} < V_o$ $I_B > 0$ $(I_C > 0, I_E > 0)$	
NPN Model								
PNP Conditions for validity	$V_{EB} < V_o$ $V_{CB} < V_o$		$\beta_F I_B > I_C$ or $\beta_R I_B > I_E$		$V_{CB} < V_o$ $I_B > 0$ $(I_C > 0, I_E > 0)$		$V_{EB} < V_o$ $I_B > 0$ $(I_C > 0, I_E > 0)$	
PNP Model								

Example:



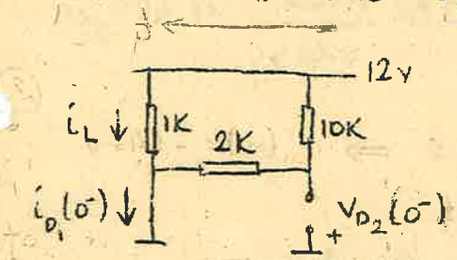


In the above circuit the diodes are ideal, and the circuit is at steady state at $t=0^-$. Find and plot $v_{o1}(t)$ and $v_{o2}(t)$ for $t \geq 0$.

Solution:

At $t=0^-$: L is short circuit (steady state)

Assume D_1 ON, D_2 OFF



$i_{D_1}(0^-) = 12 + 1 = 13\,mA > 0$ ✓

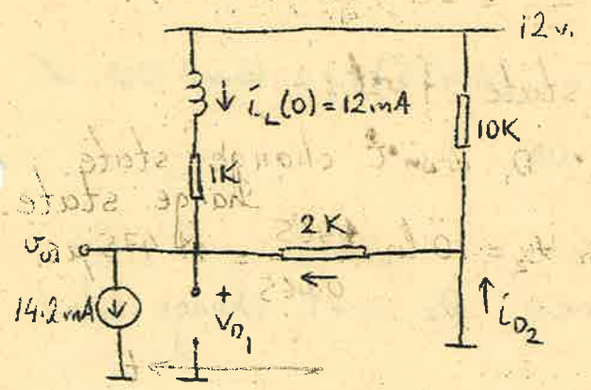
$v_{D_2}(0^-) = -2v < 0$ ✓

$\therefore$ D_1 is ON, D_2 is OFF

$i_L(0) = 12\,mA$ $\quad v_{o1}(0^-) = 0$ $\quad v_{o2}(0^-) = 2v.$

At $t=0^+$:

Assume D_1 OFF, D_2 ON



$i_{2K} = 14.2 - 12 = 2.2\,mA$

$i_{D_2}(0^+) = 2.2 - 1.2 = 1mA > 0$ ✓

$v_{D_1}(0^+) = (-2K)(2.2mA) = -4.4v < 0$ ✓

$\therefore$ D_1 is OFF, D_2 is ON

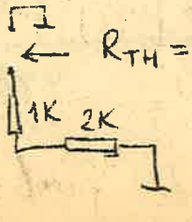
Now, solve $v_{o1}(t)$, $v_{o2}(t)$, $v_{D_1}(t)$, $i_{D_2}(t)$, $i_L(t)$ for $0 \leq t < 11.475$

$i_L(t) = 14.2 + \frac{v_{o1}(t)}{2K}\ mA$ (B) $\quad i_{D_2}(t) = -1.2 - \frac{v_{o1}}{2K}\ mA$ (A)

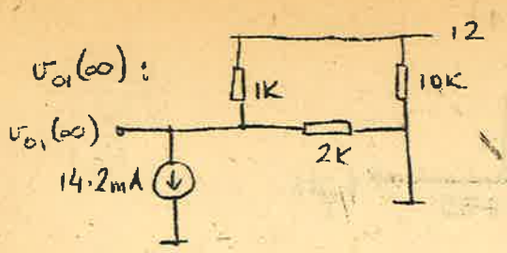
$v_{D_1}(t) = v_{o1}(t)$ $\quad v_{o2}(t) = 0.$

$v_{o1}(0^+) = -4.4v.$

τ: $\leftarrow R_{TH} = 3K$ $\quad \therefore \tau = \frac{30mH}{3K} = 10\,\mu s.$



$v_{o1}(\infty)$:



$$\frac{12 - v_{o1}}{1K} - \frac{v_{o1}}{2K} = 14.2 \Rightarrow v_{o1}(\infty) = -1.47\,v.$$

$$\therefore v_{o1}(t) = -1.47 + [-4.4 + 1.47]\,e^{-t/10} = -1.47 - 2.93\,e^{-t/10}\ v,\ \mu s.$$

$$= v_{D_1}(t)$$

From equation (A) $i_{D_2}(t) = -1.2 - \frac{v_{o1}(t)}{2} = -0.465 + 1.465\,e^{-t/10}$

Find which diode changes state first:

Observe that $v_{D_1}(\infty) = -1.47\,v < 0$. $\therefore$ D_1 won't change state.

$$i_{D_2}(t_2) = 0 = -0.465 + 1.465\,e^{-t_2/10} \Rightarrow t_2 = 10 \ln \frac{1.465}{0.465} = 11.475\,\mu s.$$

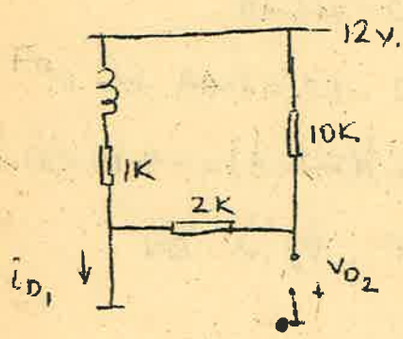
$\therefore$ D_2 becomes OFF at $t = 11.475\,\mu s$.

From equation (A) $v_{o1}(11.475) = -2.4\,v.$

" " (B) $i_L(11.475) = 14.2 - 1.2 = 13\,mA$

Replace D_2 with the OFF model and find the state of D_1 at $t = 11.475^+\,\mu s$:

Assume D_1 ON



$i_{D_1}(11.475^+) = 14\,mA$

$i_{D_1}(\infty) = 13\,mA$

$\therefore$ $i_{D_1}(t) > 0$

$\therefore$ D_1 won't change state.

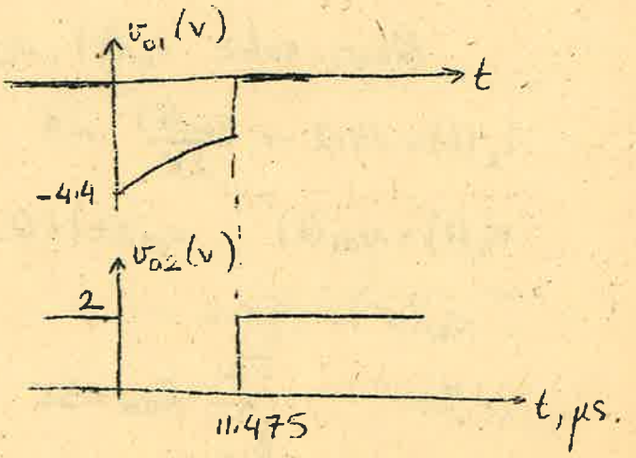
$i_{D_1}(11.475^+) = i_L(11.475) + 1 = 14\,mA > 0$ ✓

$\therefore$ D_1 is ON.

$v_{D_2}(t) = 2\,v.$

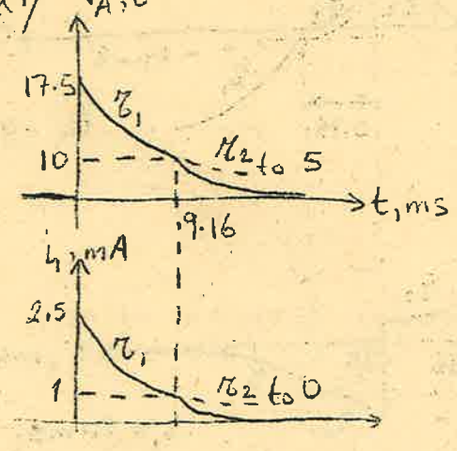
$v_{D_2}(t) = -2\,v < 0$ D_2 won't change state.

$v_{o1}(t) = 0$



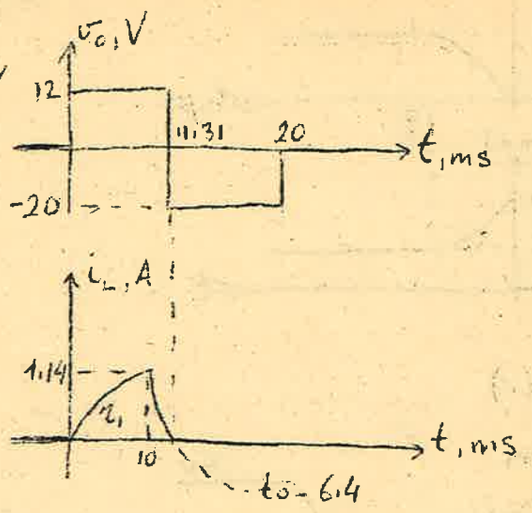
ANSWERS

Q1/



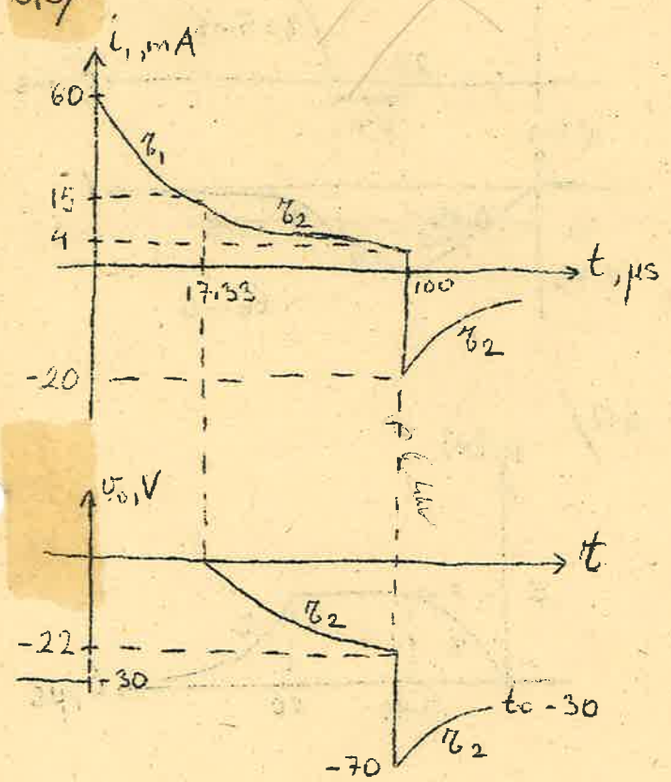
$\tau_1 = 10ms$ $\tau_2 = 15ms$

Q2/



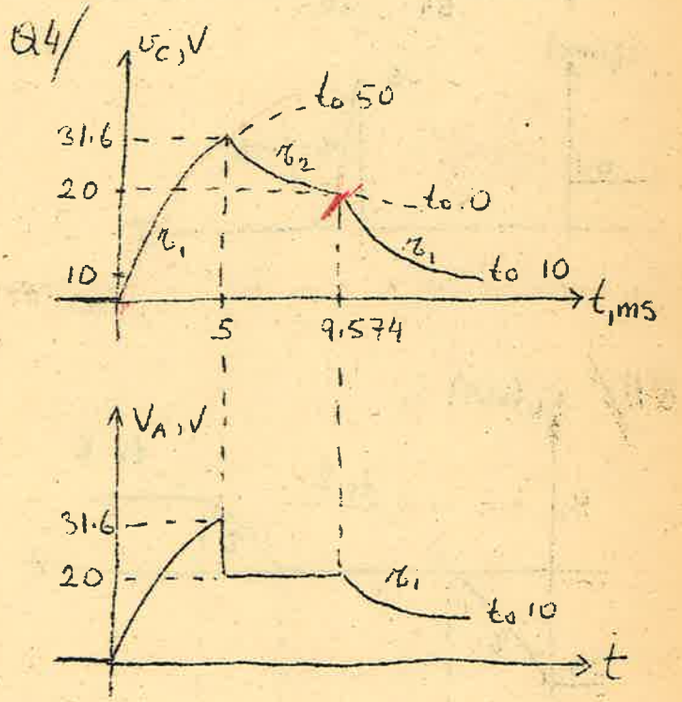
$\tau_1 = 8ms$

Q3/



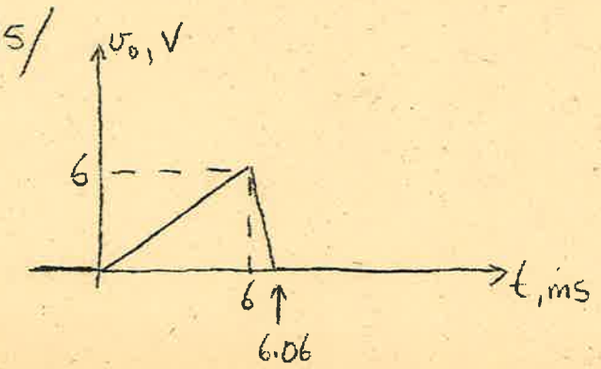
$\tau_1 = 12.5\,\mu s$ $\tau_2 = 62.5\,\mu s$

Q4/

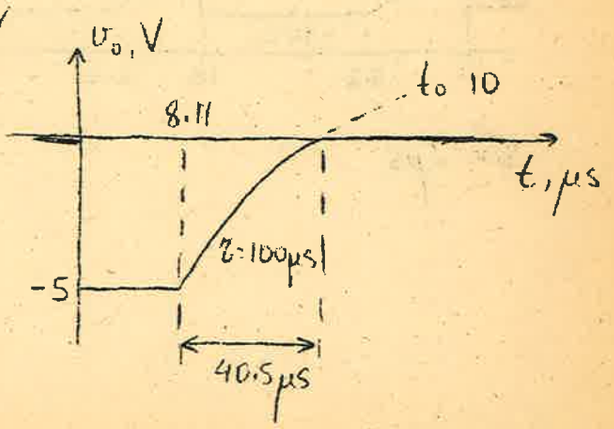


$\tau_1 = 5ms$ $\tau_2 = 10ms$

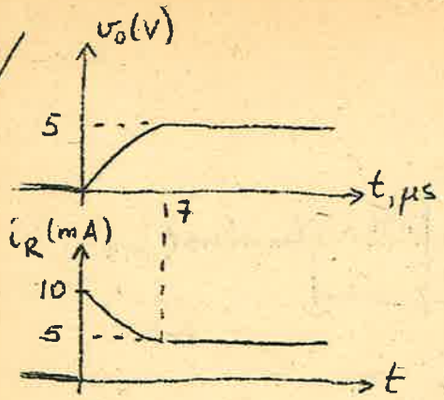
Q5/



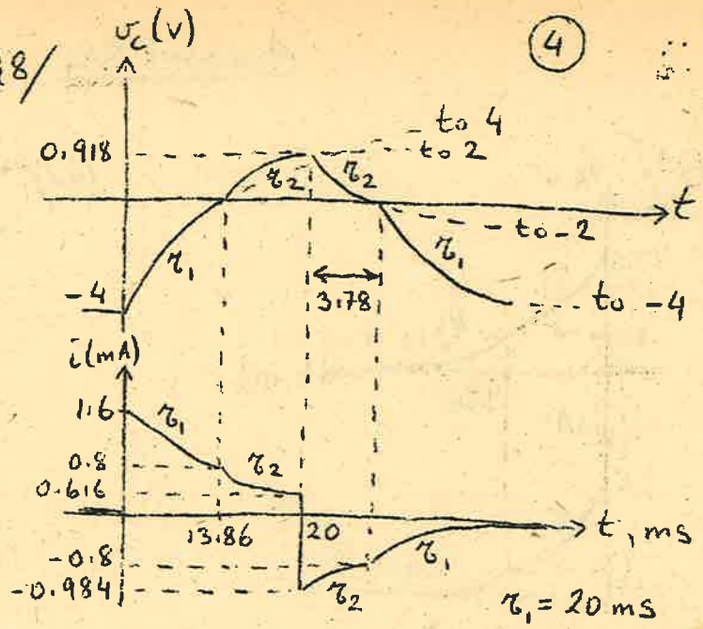
Q6/



Q7/



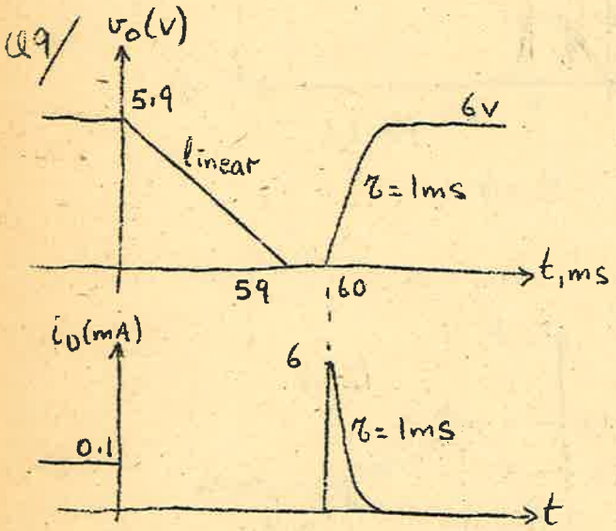
Q8/



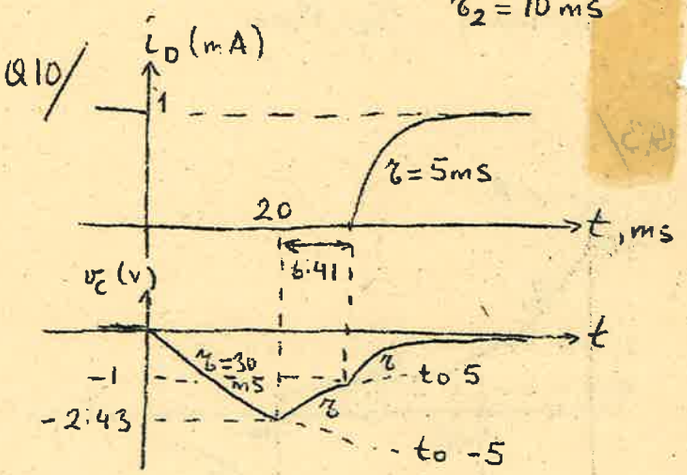
$\tau_1 = 20$ ms

$\tau_2 = 10$ ms

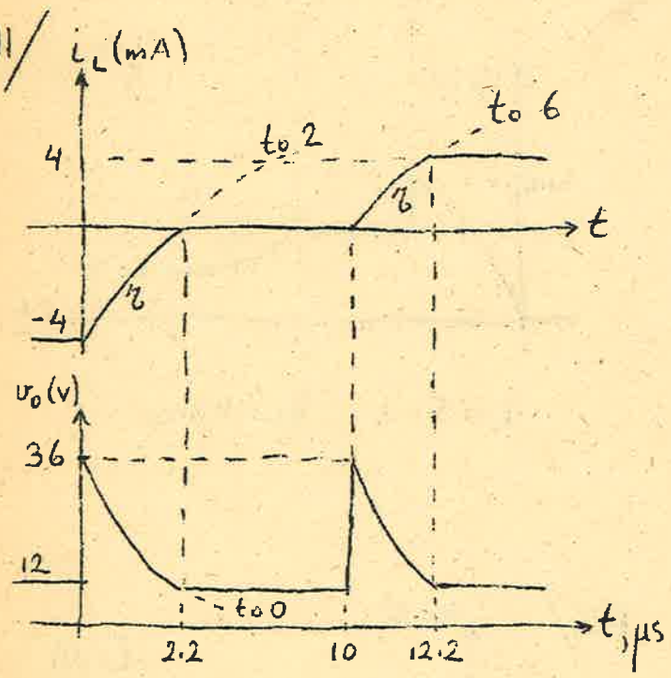
Q9/



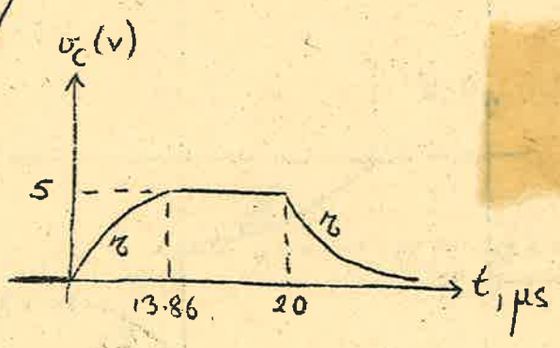
Q10/



Q11/



Q12/



$\tau = 2\,\mu s$

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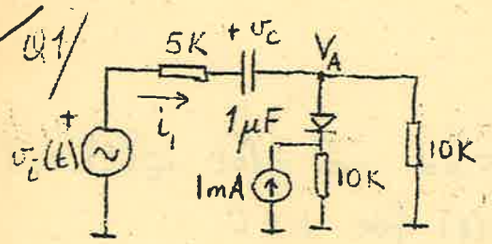
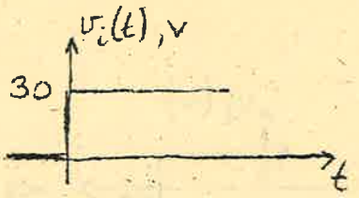
Exercise II

In all the below circuits the diodes are ideal. The circuits are at steady state at $t=0^-$.

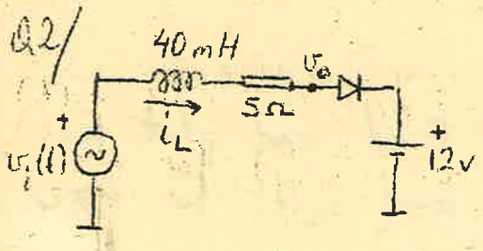
Q1/

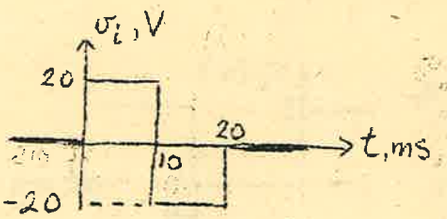




Find and plot $v_A(t)$ and $i_1(t)$ for $t \geq 0$.

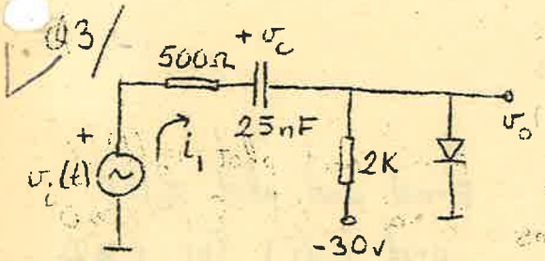
Q2/

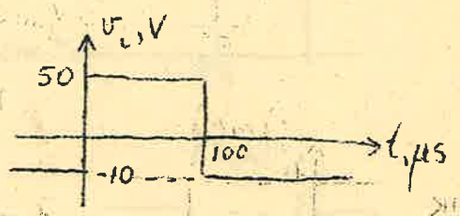




Find and plot $v_o(t)$ and $i_L(t)$ for $t \geq 0$.

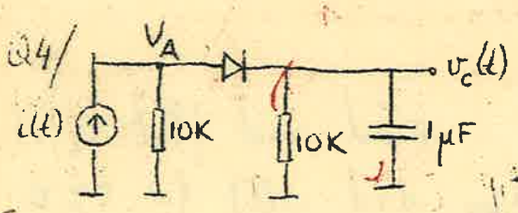
Q3/

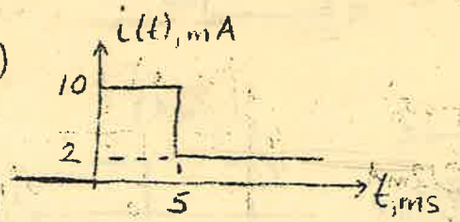




Find and plot $v_o(t)$ and $i_1(t)$ for $t \geq 0$.

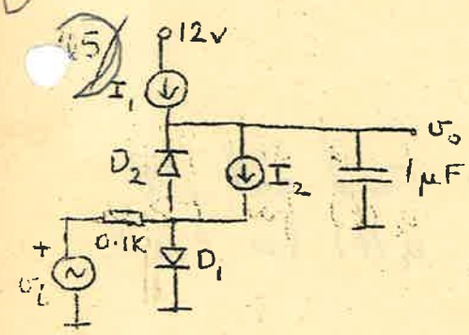
Q4/

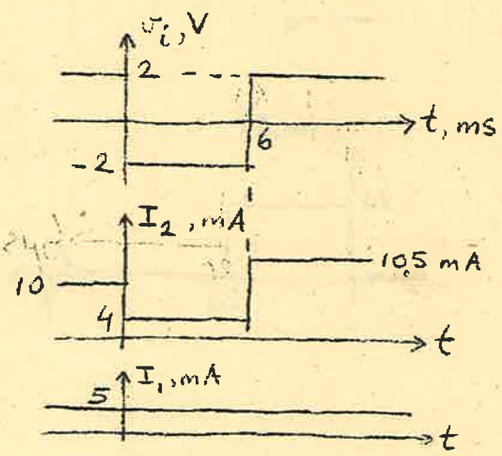




Find and plot $v_c(t)$ and $v_A(t)$ for $t \geq 0$.

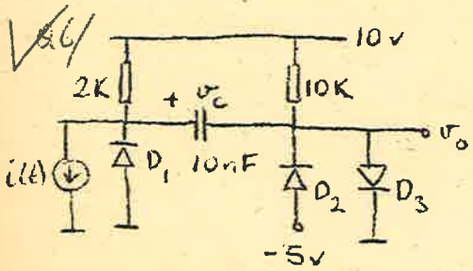
Q5/





Find and plot $v_o(t)$ for $t \geq 0$.

Q6/

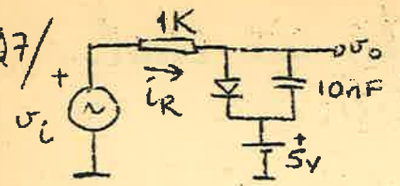


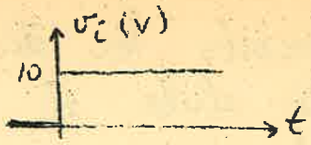
$i(t) = 0$ for $t < 0$

$i(t) = 10$ mA for $t \geq 0$

Find and plot $v_o(t)$ for $t \geq 0$.

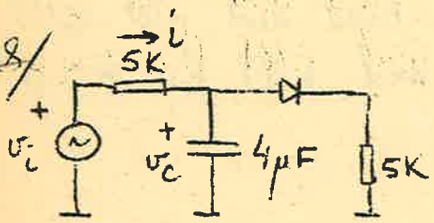
Q7/

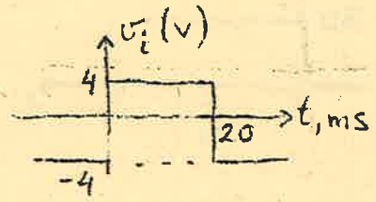




Find and plot $i_R(t)$ and $v_c(t)$ for $t \geq 0$.

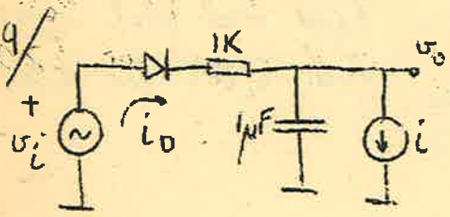
Q8/

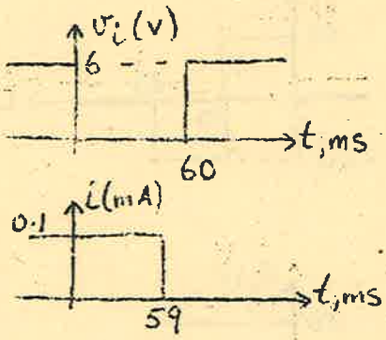




Find and plot $v_c(t)$ and $i(t)$ for $t \geq 0$.

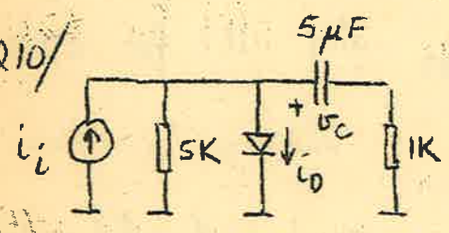
Q9/

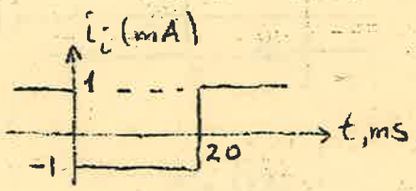




Find and plot $v_o(t)$ and $i_D(t)$ for $t \geq 0$.

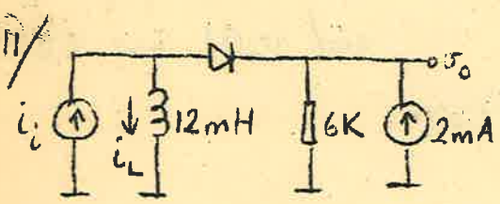
Q10/

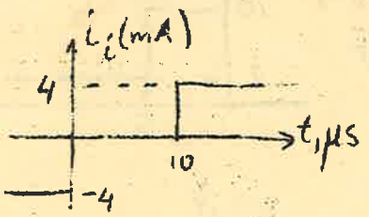




Find and plot $v_c(t)$ and $i_D(t)$ for $t \geq 0$.

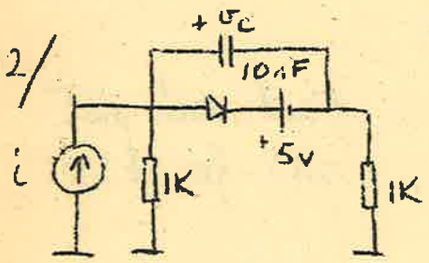
Q11/

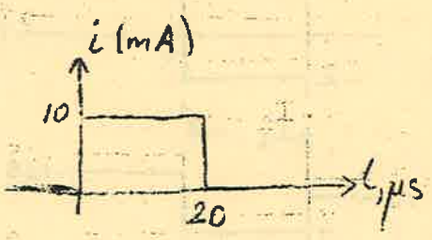




Find and plot $i_L(t)$ and $v_o(t)$ for $t \geq 0$.

Q12/

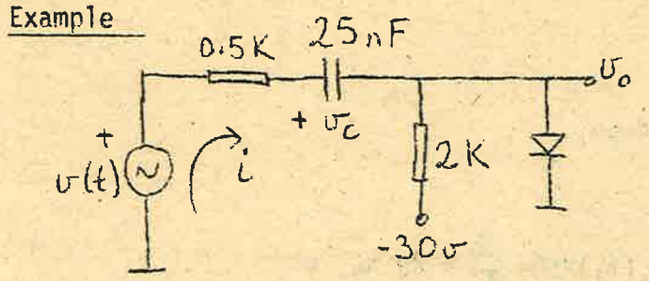


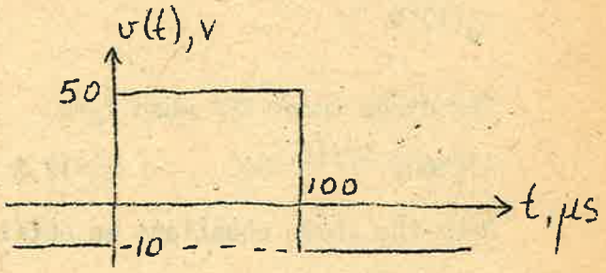


Find and plot $v_c(t)$ for $t \geq 0$.

An Example on Piecewise Linear Solution of Networks Containing Single Energy Storage Element

Example



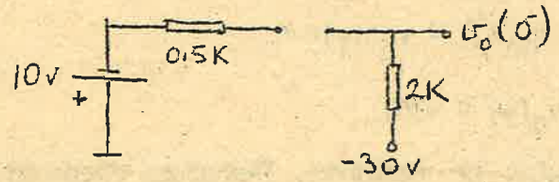


In the above circuit assume that the diod-e is ideal and the circuit is at steady state at $t = 0^-$. Find and plot $v_0(t)$ and $i(t)$ for $t>0$.

Solution:

Find the state of the diode at $t=0^-$:

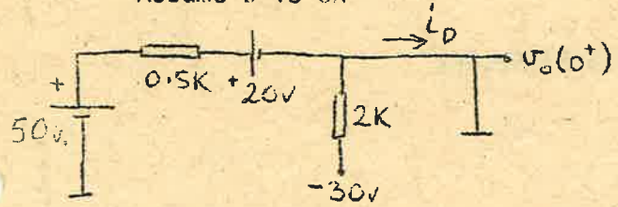
Since the circuit is at steady state at $t=0^-$, C is open circuit. Remove C, assume D is OFF. Then V_D= -30v. Therefore D is OFF.



$v_0(0^-) = -30$ v.
$i(0^-) = 0$.
$v_c(0^-) = 20$v.

Now, find the state of the diode at $t=0^+$:

Assume D is ON



$i_D(0^+) = \frac{50-20}{0.5} - \frac{30}{2} = 45\text{mA} > 0.$

Therefore D is ON.

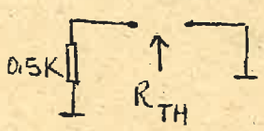
Find the initial values:

$i_D(0^+) = 45$mA
$v_0(0^+) = 0$
$i(0^+) = 50$ mA
$v_c(0) = 20$v

Find the steady state values:

(C is open)
$i_D(\infty) = -15$mA
$v_0(\infty) = 0$
$i(\infty) = 0$
$v_c(\infty) = 50$v

Find the time constant:



$\tau = (0.5K)(25nF)$
$= 12.5\ \mu s.$

$i_D(t) = -15+60e^{-t/12.5}$ mA,μs $i(t)=60e^{-t/12.5}$ mA,μs.

$v_o(t)=0$ $v_c(t)=50-30e^{-t/12.5}$ V,μs.

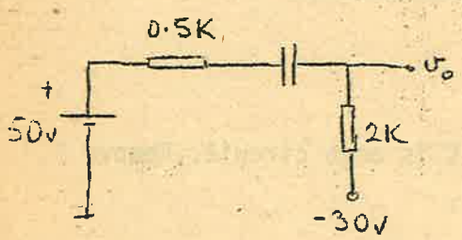
The diode turns OFF when $i_D=0$.

$-15+60e^{-t_1/12.5}=0$ $t_1=12.5 \ln 4$ μs.

From the above equations we obtain

$i(t_1^-)= \frac{60}{4} = 15$ mA ✓ $v_c(t_1)=50-\frac{30}{4} = 42.5$v. ✓

For $t_1<t<100$μs, replace the diode with the OFF model:



$v_c(t_1)=42.5$v.

$v_o(t_1^+) = \frac{80-42.5}{2.5} .2-30 = 0.$

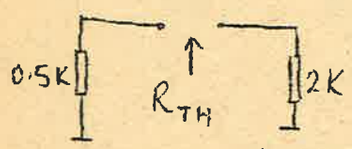
$i(t_1^+)= \frac{v_o(t_1^+)+30}{2} = 15$ mA

$v_D(t_1^+) = v_o(t_1) = 0.$

$i(\infty)=0$, $v_c(\infty)= 80$v., $v_o(\infty)=30$v., $v_D(\infty) = -30$v.

Since $v_D(t_1) =0$ and $v_D(\infty)=-30$v, $v_D(t)$ is negative. Therefore diode will not change state.

Find the time constant:



$\tau = (2.5K).(25nF)=62.5\mu s$

$v_c(t)=80-37.5e^{-(t-12.5\ln 4)/62.5}$ v,μs.

$i(t)=15e^{-(t-12.5\ln 4)/62.5}$ mA,μs.

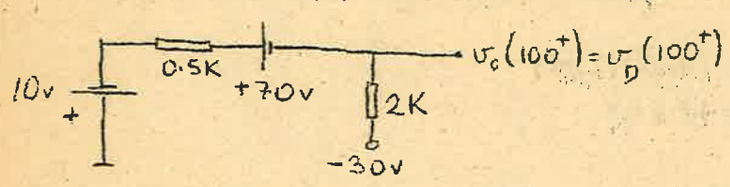
From the above equations we obtain

$v_c(100\ s) = 70$ v.

$i(100^-s) = 4$ mA

$v_o(100^-\mu s)=-30+2x4 = -22$v.

For $t>100$μs, $v(t)=-10$v. Assume D OFF.



$v_D(100^+)=-30-\frac{50}{2.5}x2 = -70v<0$

Therefore diode is OFF.

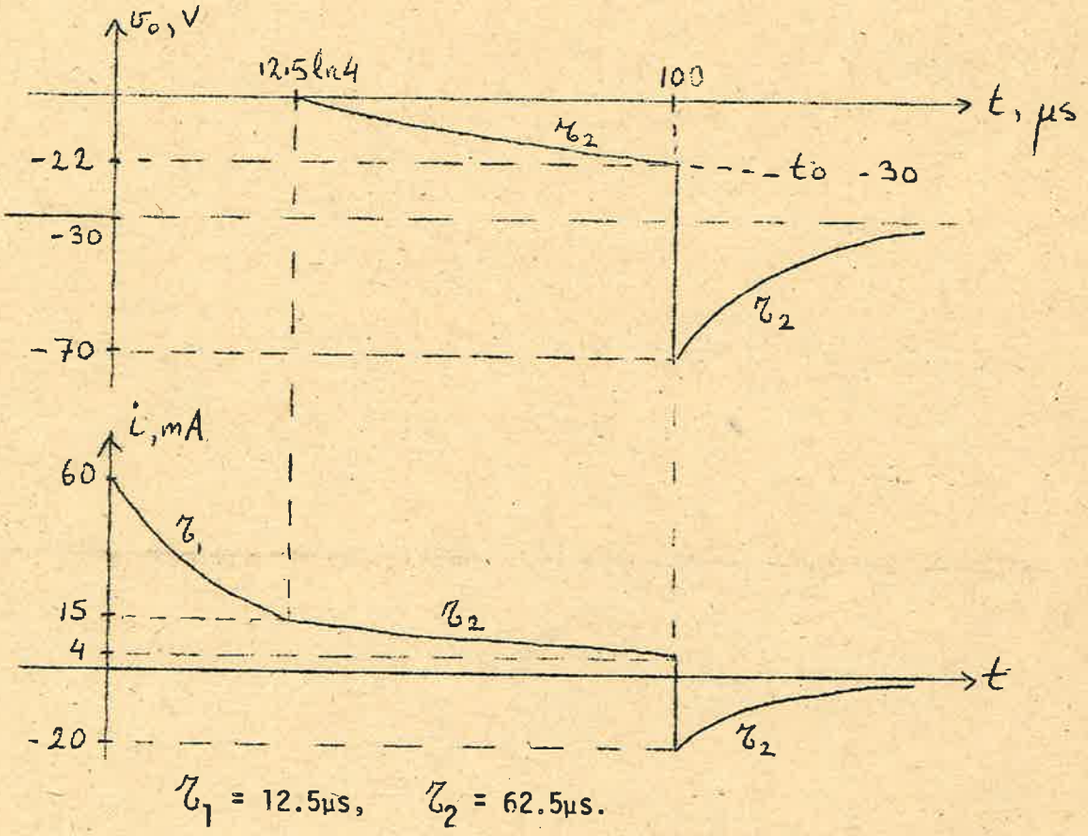
$v_o(100^+s) = -70v. = v_D(100^+)$

$i(100^+\mu s) = \dfrac{v_o(100^+)+30}{2} = -20mA$

$v_D(\infty) = -30v.$ Therefore the diode remains OFF ($v_D(100^+)$ is also negative)

$v_o(\infty) = -30v.$

$i(\infty) = 0.$



$\tau_1 = 12.5\mu s, \quad \tau_2 = 62.5\mu s.$

$y(t) = y(\infty) + [y(0) - y(\infty)]\, e^{-t/\tau}$

$\tau = R_{th} C$

$\tau = \frac{L}{R_{th}}$

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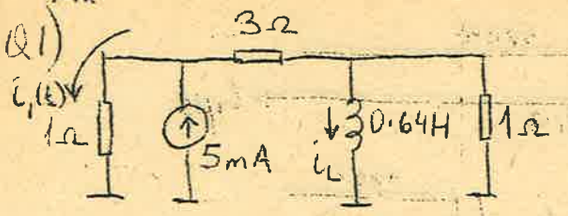
EXERCISE 1

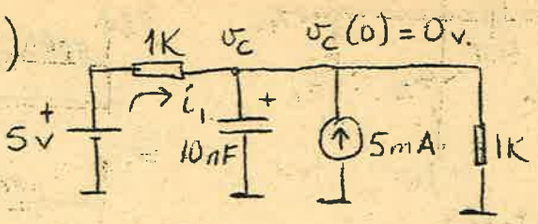
Q1)



$i_L(0) = 2\text{mA}$

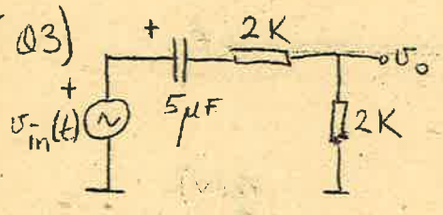
Find and plot $i_L(t)$ and $i_1(t)$

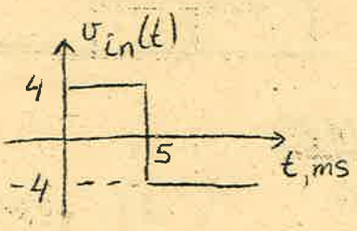
Q2)



Find and plot $i_1(t)$ and $v_c(t)$.

Q3)

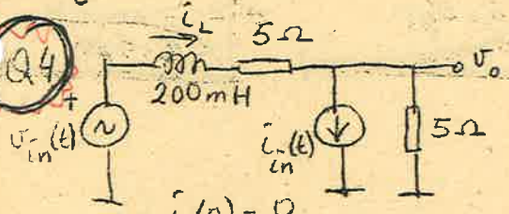




Find and plot $v_o(t)$.

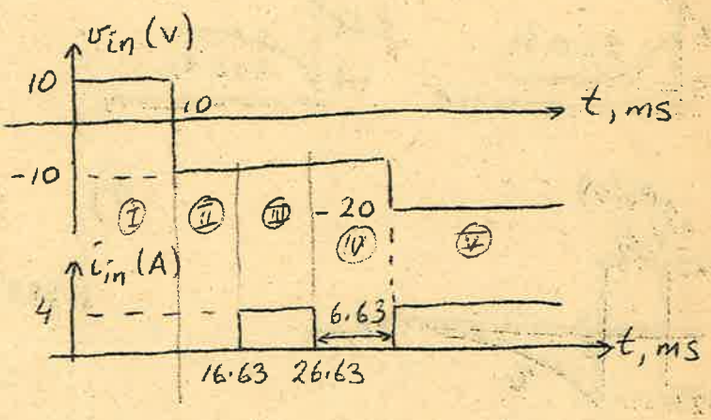
$v_c(0) = 2\text{v}$

Q4)

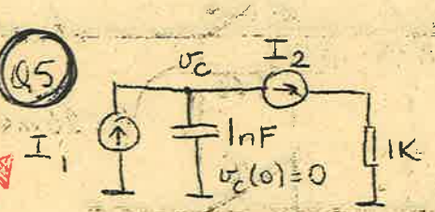


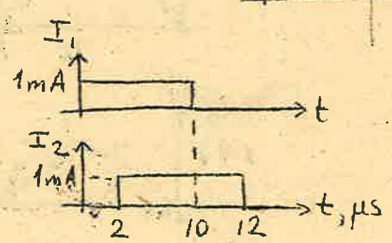
$i_L(0) = 0$

Find and plot $i_L(t)$ and $v_o(t)$



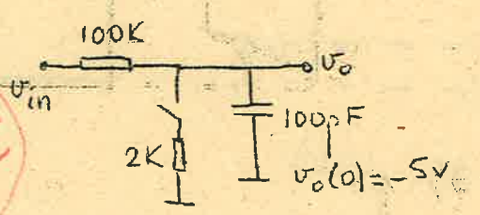
Q5)

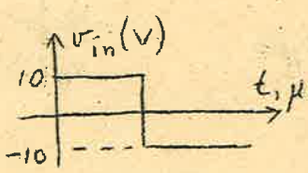




Find and plot $v_c(t)$.

Q6)





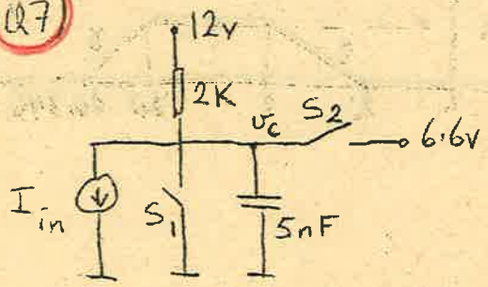
The switch automatically closes whenever the output voltage is positive and opens when it is negative.

Find and plot $v_o(t)$

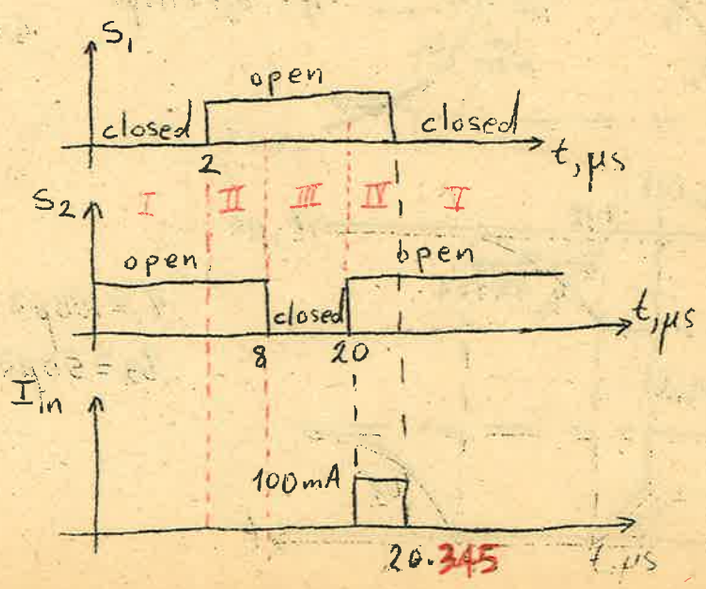
$V_1 - V_1 = \frac{Q}{C}$

$Q = \int i\, dt$

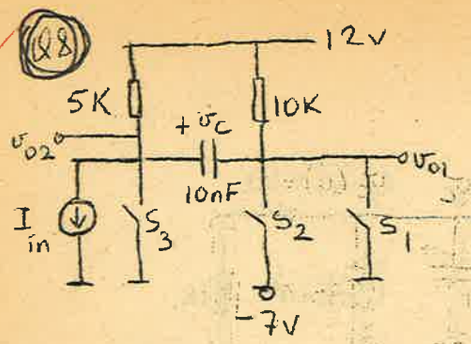
Q7)



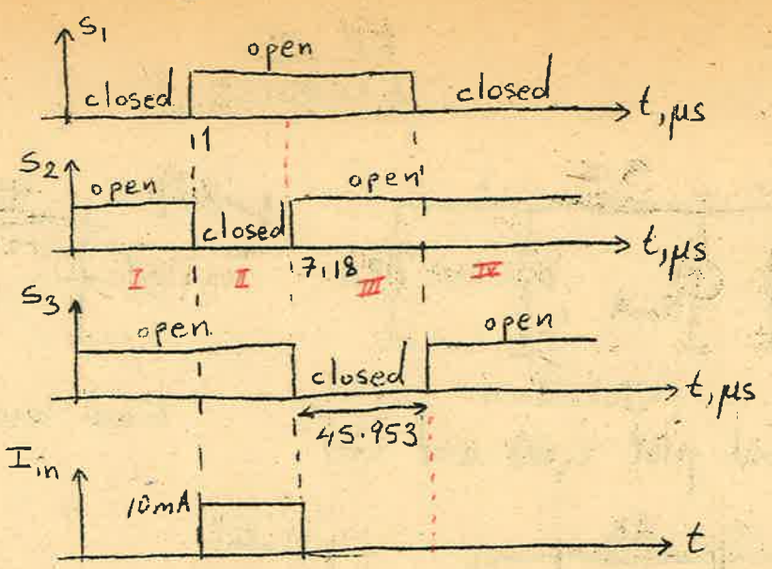
Find and plot $v_c(t)$.



(8)

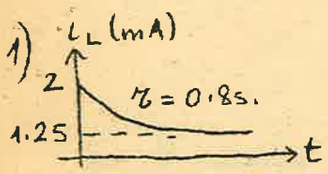


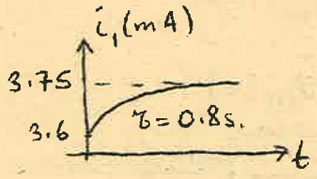
$v_C(0) = 12$ V.



ANSWERS

1)





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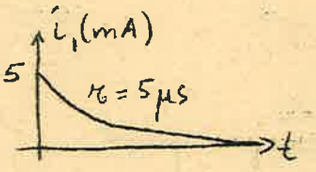
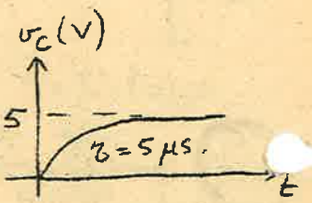
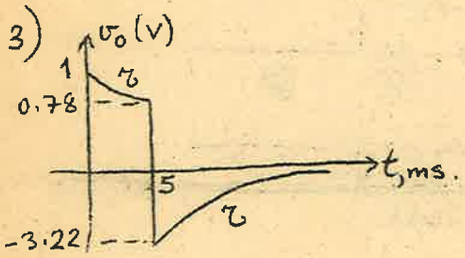


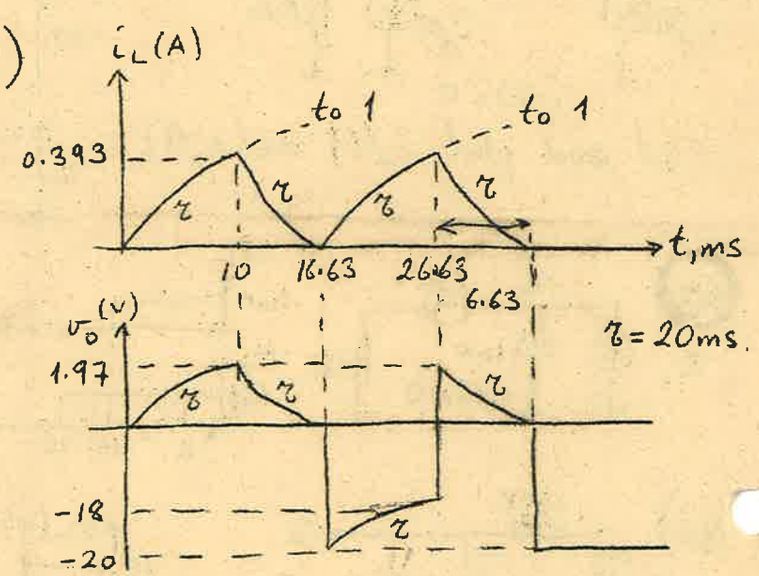


3)

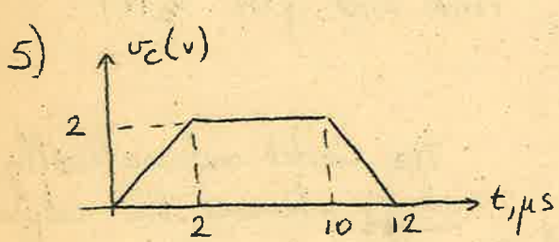


$\tau = 20$ms.

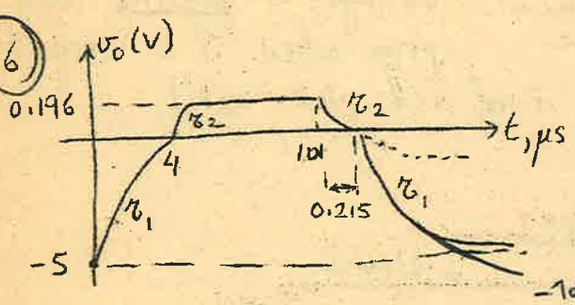
4)



5)



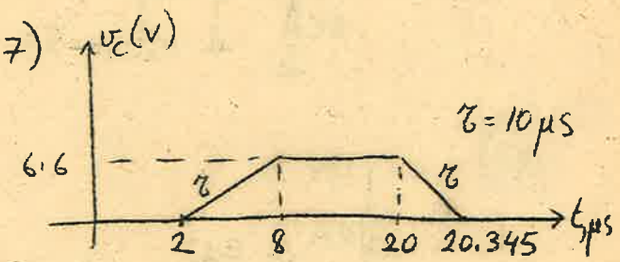
6)



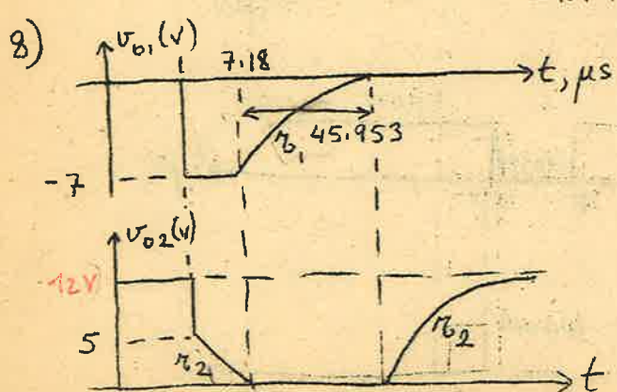
$\tau_1 = 10\mu$s

$\tau_2 = 0.196\mu$s

7)



8)

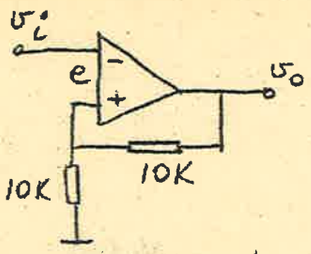


$\tau_1 = 100\mu$s

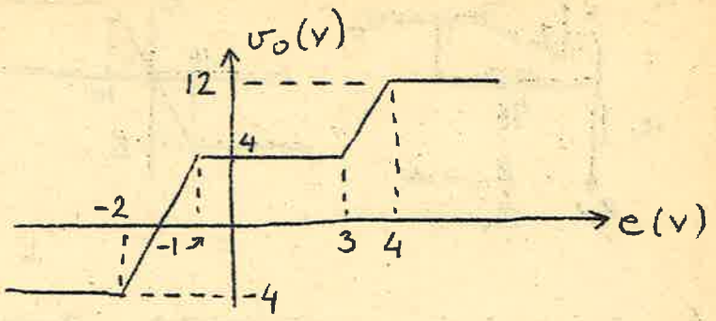
$\tau_2 = 50\mu$s

EE 411
EXERCISE

Q1

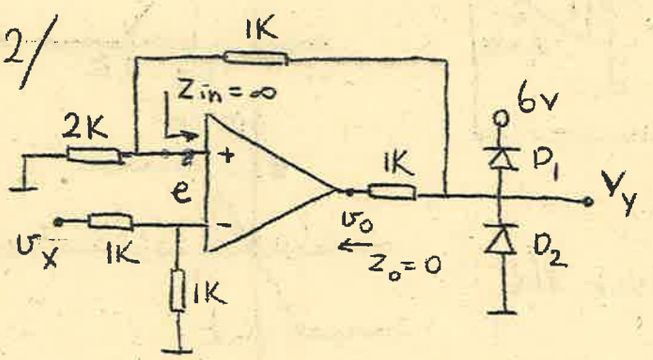


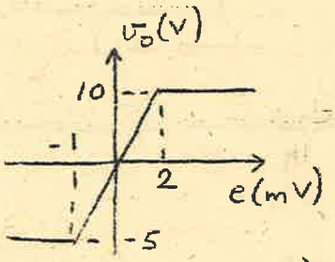
The amplifier is ideal
$Z_{in} = \infty$, $Z_o = 0$.



Obtain and sketch v_o vs. v_i.

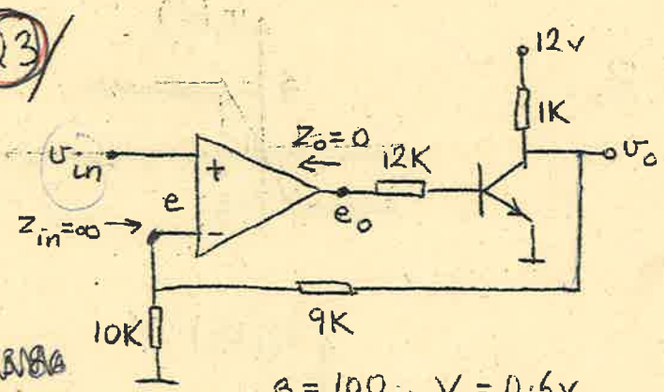
Q2



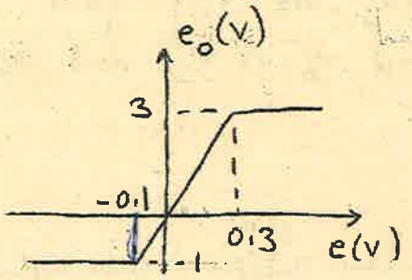


Both diodes are ideal.
a) Find the loop gain
b) Find and plot V_y vs. V_x.

Q3

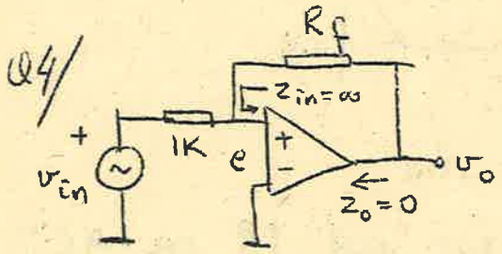


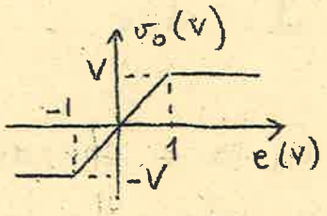
$\beta = 100$, $V_o = 0.6$V

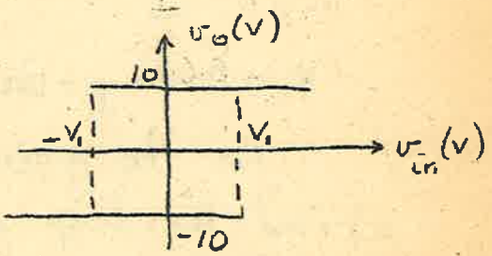


a) Find the loop gain. Find the range of 'e' for which TR is ACT.
b) Calculate and plot the transfer characteristic v_o vs. v_{in}.

Q4

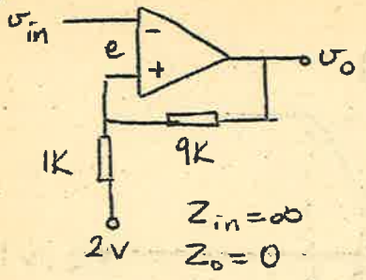




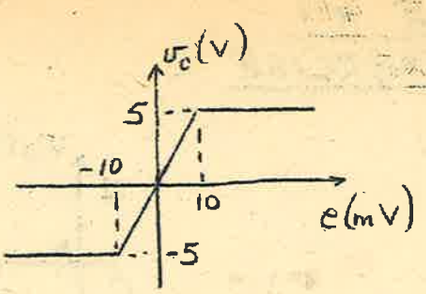


Given A_L (loop gain) = 5 and the above characteristics find V, V_1, R_f.

Q5/

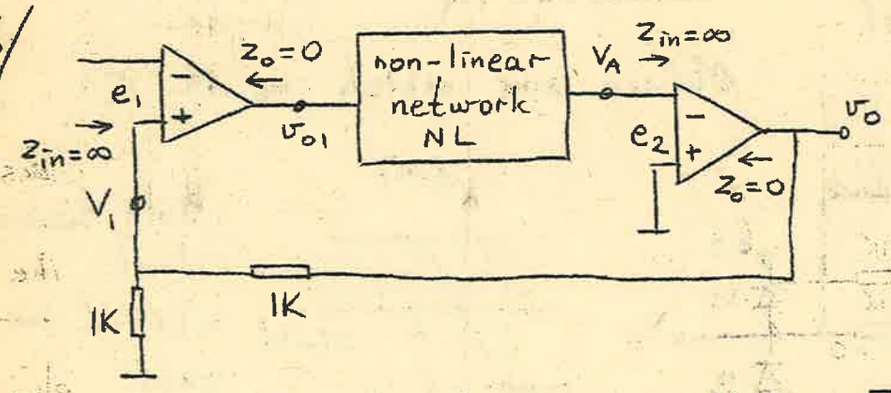


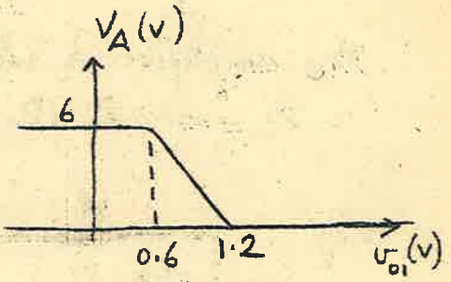
$Z_{in}=\infty$
$Z_o=0$

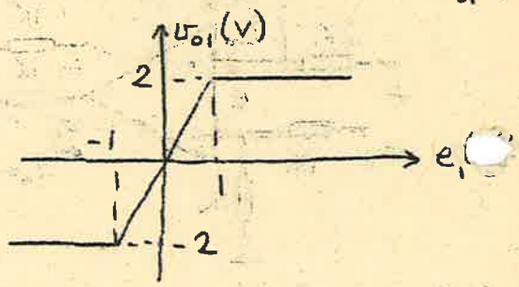


Plot v_o vs. v_{in}.

Q6/



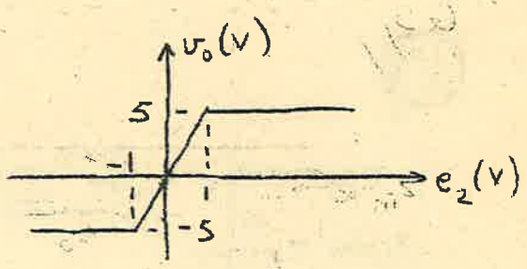




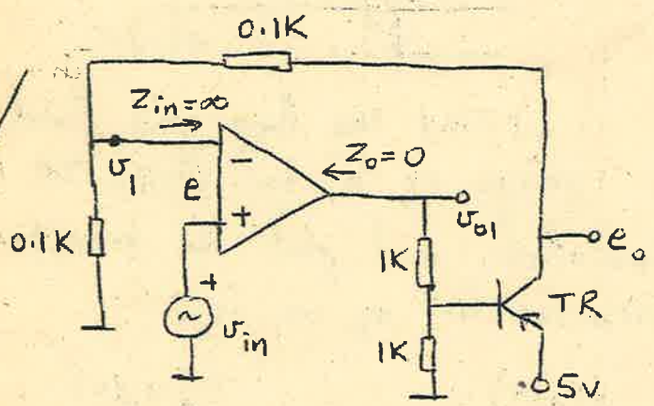
The amplifiers and NL have the given characteristics.

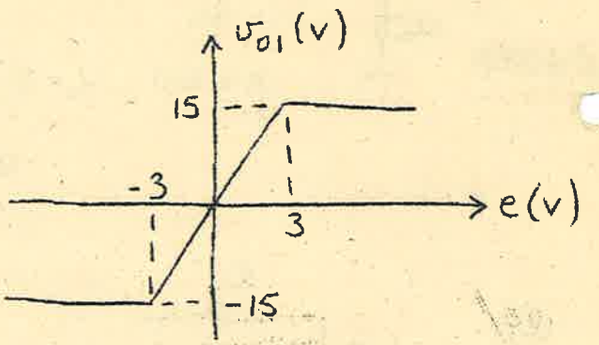
a) Find the loop gain

b) Find v_A vs. v_{in} and v_o vs. v_{in}.



Q7/





$V_o = 0.6V$ $\beta = 100$

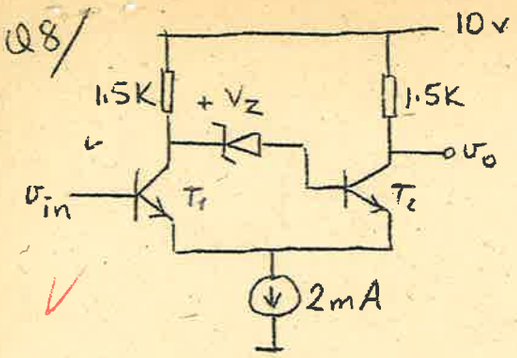
For the given v_{01} vs. e characteristic

a) Find the loop gain when the amplifier and TR are ACT.

b) Find the region of v_{01} for which TR is ACT

c) Find and sketch v_{01} vs. v_{in} and e_o vs. v_{in} for $-\infty \leq v_{in} \leq \infty$.

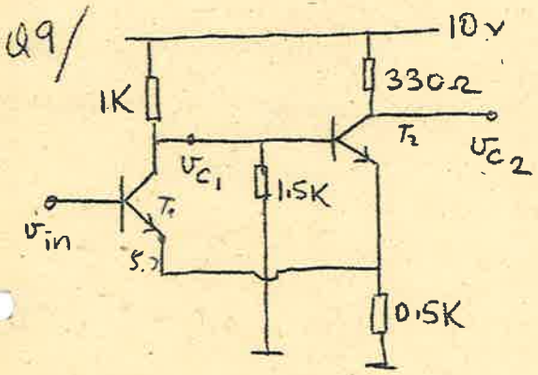
Q8/



Find the transfer characteristic v_o vs. v_{in} for $0 < v_{in} < 10v$.

$\beta = 100$, $V_o = 0.6v$, $V_z = 5v$

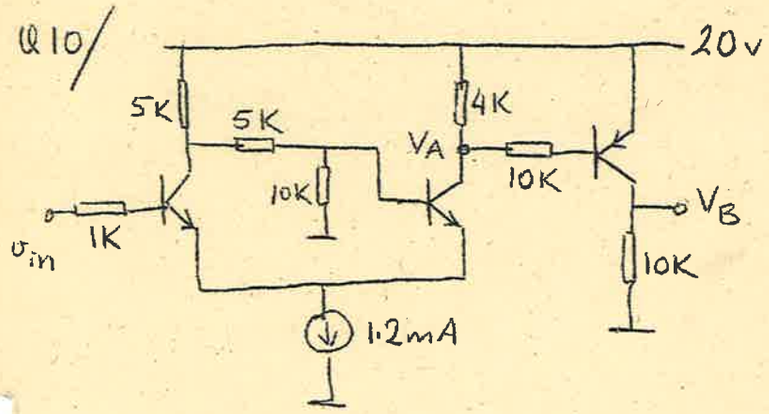
Q9/



Plot v_{C_1} and v_{C_2} vs. v_{in} for $0 \le v_{in} \le 10$

$\beta = 100$, $V_o = 0.6v$

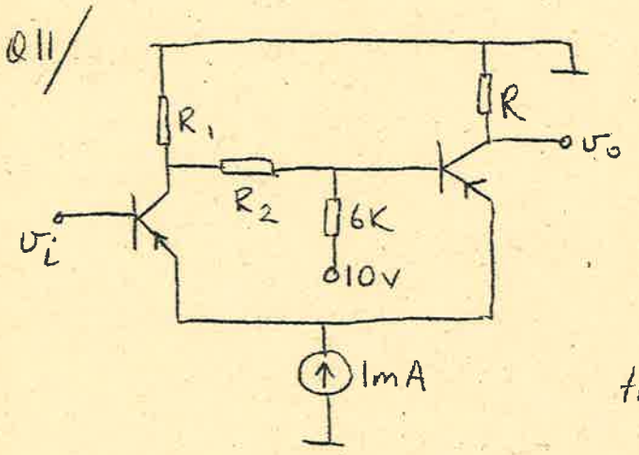
Q10/

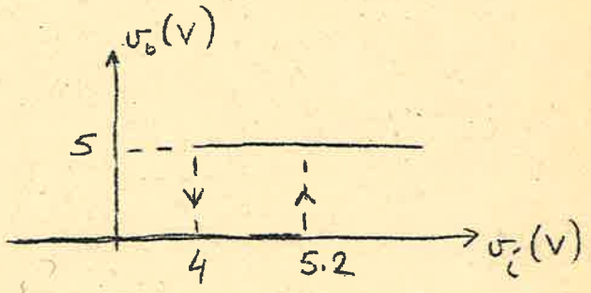


Find and plot V_A and V_B vs. v_{in}

$\beta = 100$, $V_o = 0.6v$

Q11/



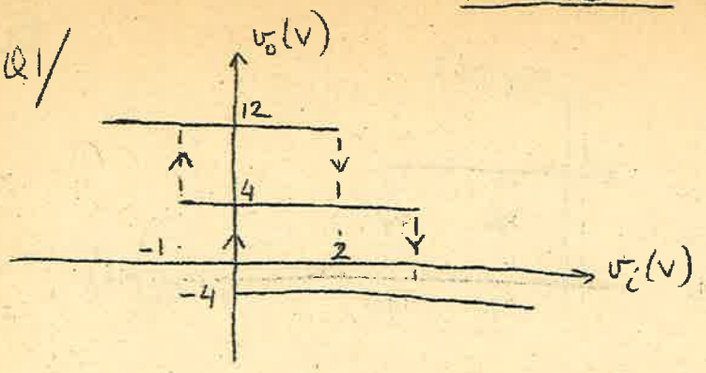


Determine R, R_1 and R_2 so that the above characteristic is obtained.

$\beta = 50$, $V_o = 0.6v$

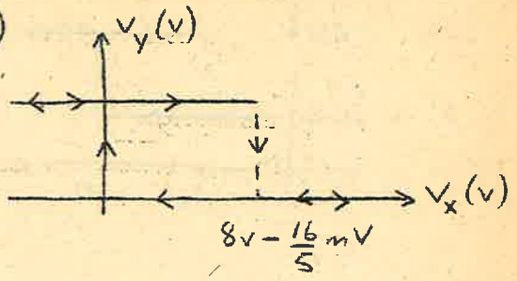
ANSWERS

Q1/



Q2/ a) $A_L = 2500$

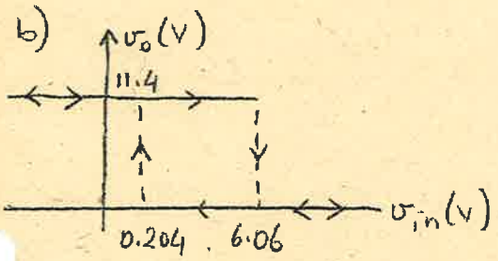
b)



Q3/ a) $A_L \simeq 41.7$

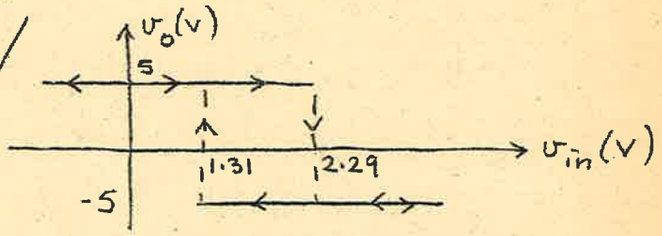
$0.06 < e < 0.204$

b)



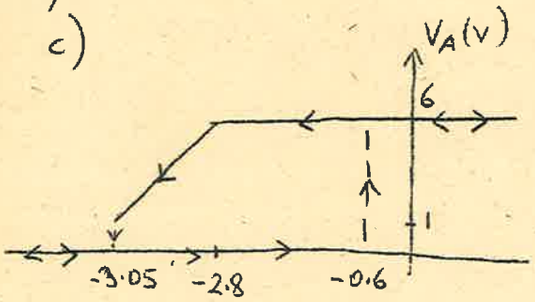
Q4/ $V = 10v$, $V_1 = 8v$, $R_f = 1K$

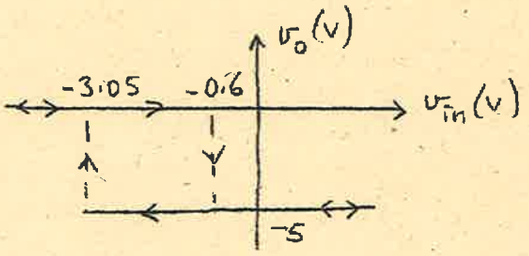
Q5/



Q6/ a) $A_L = 50$

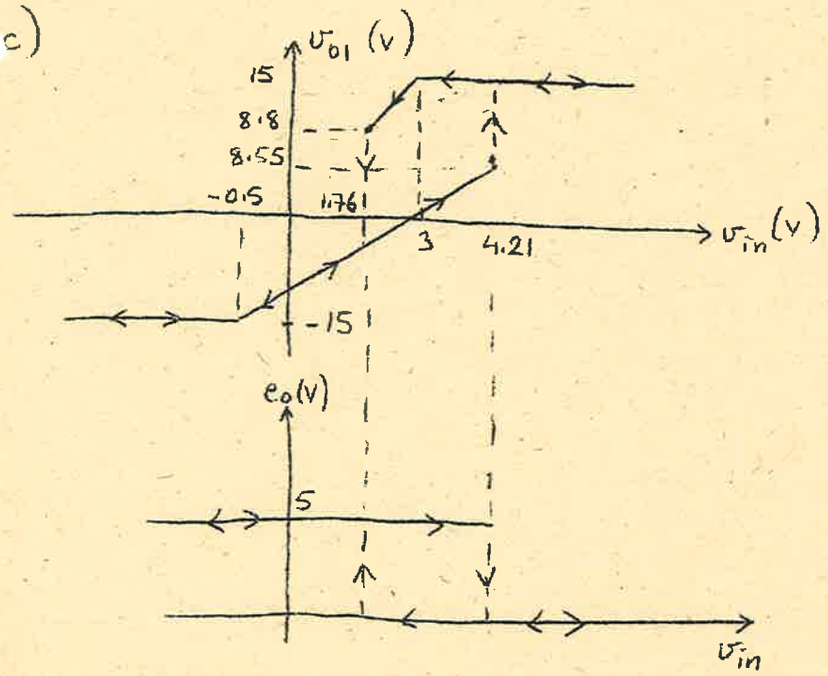
c)



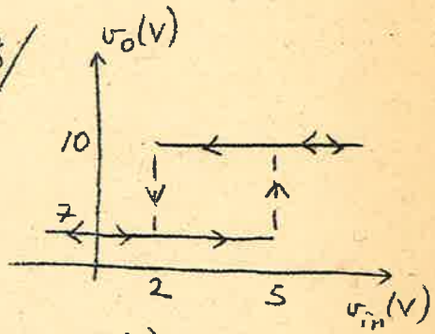


Q7/ a) $A_L = 50$ b) $8.55v \leq v_{01} \leq 8.8v$

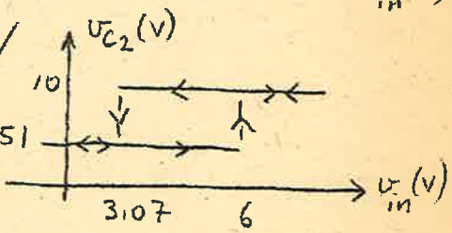
c)

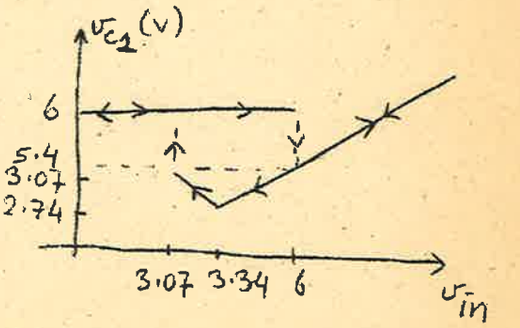


Q8/

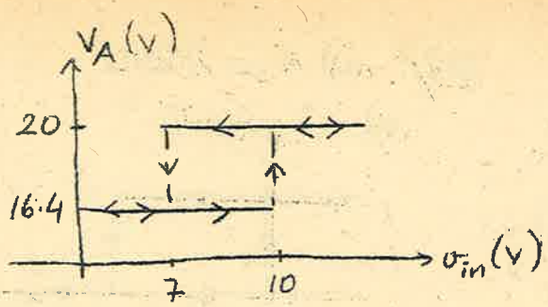


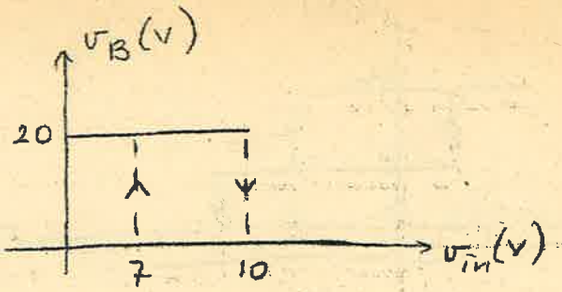
Q9/





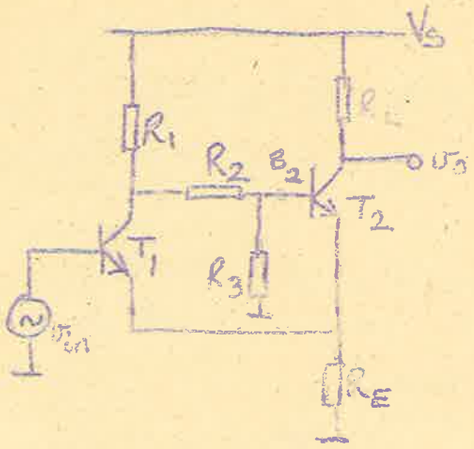
Q10/





Q11/ $R = 5.1K$, $R_1 = 1.8K$, $R_2 = 2.12\ K$

Schmitt Trigger Circuit (A regenerative comparator)

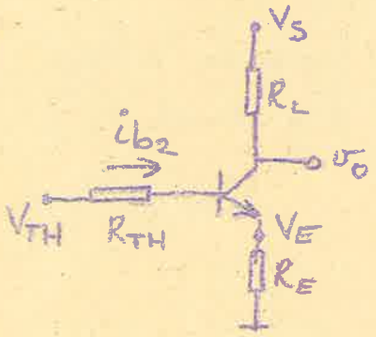


Assume $v_{in} = -\infty$. Then T_1 is OFF.

Find Thevenin equivalent circuit at B_2:

$$V_{TH} = \frac{V_S R_3}{R_1 + R_2 + R_3} \qquad R_{TH} = (R_1 + R_2) \,//\, R_3$$

Therefore we have:



T_2 is designed to be ACT.

$$i_{b_2} = \frac{V_{TH} - V_o - V_E}{R_{TH}} \quad (1) \qquad i_{e_2} = (\beta_2 + 1) i_{b_2}$$

$$V_E = (\beta_2 + 1) i_{b_2} R_E$$

$$\therefore i_{b_2} = \frac{V_E}{(\beta_2 + 1) R_E} \quad (2)$$

From (1) and (2) we obtain:

$$V_E = \frac{(\beta_2 + 1)(V_{TH} - V_o) R_E}{R_{TH} + (\beta_2 + 1) R_E} \triangleq V_{E2} \quad (3)$$

Inorder to have T_2 ACT, one must satisfy the condition

$$v_{CE2} > 0 \quad (\text{assuming } V_{CE2\,SAT} = 0)$$

$$v_{CE2} = V_S - R_L i_{C_2} - V_{E2} = V_S - \frac{R_L \beta_2}{\beta_2 + 1} i_{E2} - V_{E2}$$

$$= V_S - \frac{R_L \beta_2}{\beta_2 + 1} \cdot \frac{V_{E2}}{R_E} - V_{E2}$$

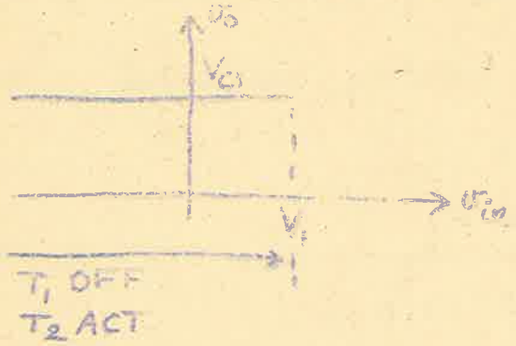
Substituting V_{E2} from (3), one can check if $v_{CE2} > 0$.

T_1 remains OFF for $v_{BE1} < V_o$ or $v_{in} - V_{E2} < V_o$

or $v_{in} < V_o + V_{E2} \triangleq V_1$

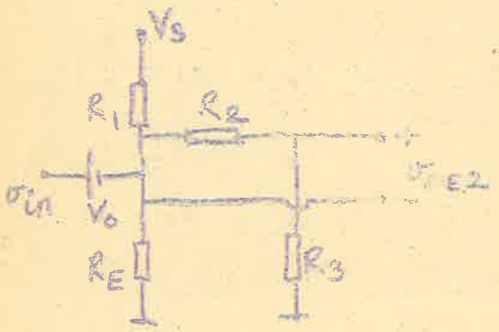
Using (3) we obtain $V_1 = V_o + \frac{(\beta_2 + 1)(V_{TH} - V_o) R_E}{R_{TH} + (\beta_2 + 1) R_E}$

or $$V_1 = V_0 + \frac{(V_{TH} - V_0) R_E}{R_E + \frac{R_{TH}}{\beta_2 + 1}} \quad (4)$$



$v_o = V_S - R_L i_{C2} \triangleq V_{C1}$

Assume now v_{in} is large positive so that T_1 is SAT, T_2 is OFF.

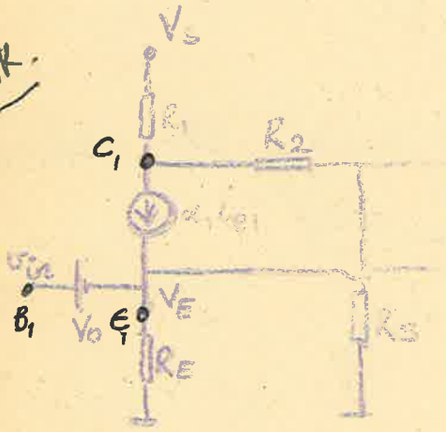


Since $v_{BE2} < 0$ (due to voltage drop across R_2)

T_2 is OFF.

Decrease v_{in} until T_1 becomes ACT. Now, we have

ACTIVE TR.
$V_{CE} > 0$



$$V_{B2} = \underbrace{\frac{V_S R_3}{R_1 + R_2 + R_3}}_{V_{TH}} - \frac{\alpha_1 i_{e1} R_1 R_3}{R_1 + R_2 + R_3}$$

$V_E = i_{e1} R_E$

$$\therefore V_{BE2} = V_{TH} - \frac{\alpha_1 V_E R_1 R_3}{R_E (R_1 + R_2 + R_3)} - V_E \quad (5)$$

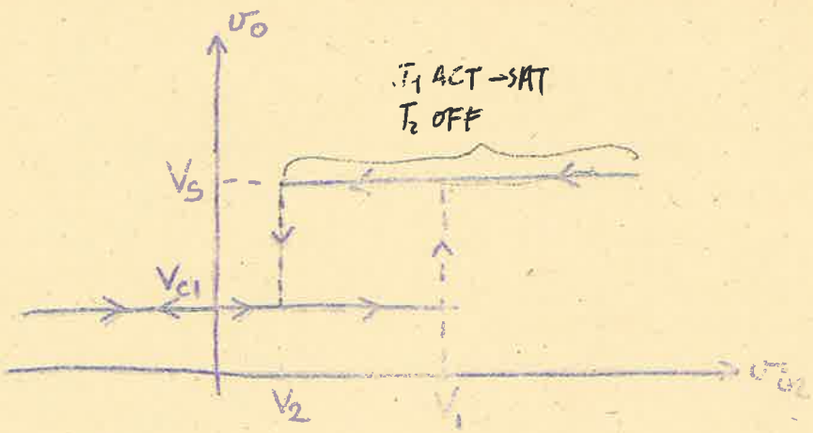
For $v_{BE2} < V_0$, T_2 is OFF and $v_o = V_S$.

From (5) $v_{BE2} < V_0 \Rightarrow V_E > \dfrac{(V_{TH} - V_0) R_E}{R_E + \dfrac{\alpha_1 R_1 R_3}{R_1 + R_2 + R_3}}$

Since $V_E = v_{in} - V_0$, T_2 is OFF for

$$v_{in} > V_0 + \frac{(V_{TH} - V_0) R_E}{R_E + \dfrac{\alpha_1 R_1 R_3}{R_1 + R_2 + R_3}} \triangleq V_2 \quad (6)$$

Therefore we have



Inorder to have a hysteresis characteristic we must have $V_1 > V_2$.

Comparing equations (6) and (4), $V_1 > V_2$ if

$$\frac{R_{TH}}{\beta_2 + 1} < \frac{\alpha_1 R_1 R_3}{R_1 + R_2 + R_3} \qquad \text{where } R_{TH} = \frac{(R_1 + R_2) R_3}{R_1 + R_2 + R_3}$$

$$\therefore \frac{(R_1 + R_2) R_3}{(R_1 + R_2 + R_3)(\beta_2 + 1)} < \frac{\alpha_1 R_1 R_3}{(R_1 + R_2 + R_3)}$$

$\alpha_1 (\beta_2 + 1) R_1 > R_1 + R_2$. This is a necessary condition to have $A_L > 1$.

EE 411

SUPPLEMENTARY NOTE

COLLECTOR COUPLED ASTABLE MULTIVIBRATOR

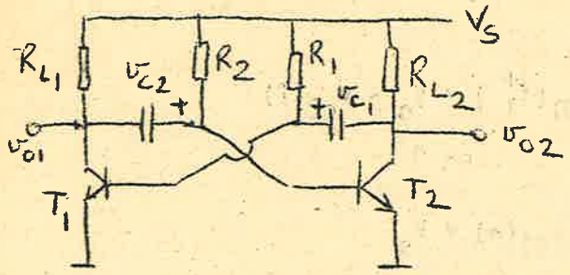


Fig.1

As seen from the figure the astable can be considered as two monostable circuits operating sequentially, one triggered off when the other one turns on. The circuit is self starting and free running.

There are two quasi-stable (pulse) states:

1) T_1OFF, T_2SAT 2) T_1SAT, T_2 OFF

Suppose at $t=0^-$ T_1 is OFF, T_2 is SAT:

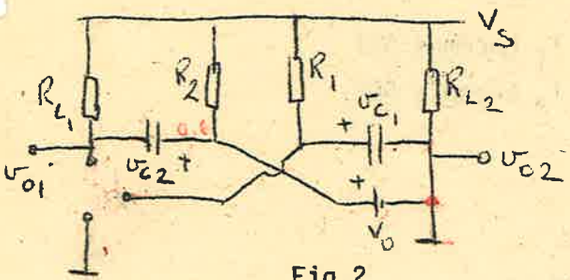


Fig.2

Assume at t=0 regeneration is just starting. Then we must have

$v_{c1}(0) = v_{B_1}(0^-) = V_0$.

$v_{c2}(0) = -V_s+V_0$ (steady state)

Then $v_{01}(0^-) = V_s$, $v_{02}(0^-) = 0$.

Since at t=0 we have regeneration T_1 becomes SAT, T_2 becomes OFF.

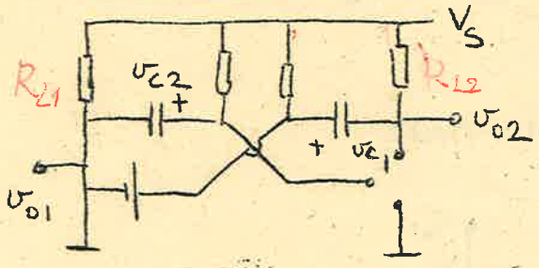


Fig.3

$V_{01} = 0$ $v_{02}(0^+) = V_0 - v_{c1}(0) = 0$

$v_{02}(\infty) = V_s$ $\tau_1 = R_{L2}C_1$

$v_{B1} = V_0$ $v_{B_2}(0^+) = v_{c2}(0) = -V_s+V_0$

$v_{B_2}(\infty) = V_s$ $\tau_2 = R_2C_2$

Usually $\tau_1 \ll \tau_2$

$$v_{B_2}(t) = V_s+(-2V_s+V_0)\, e^{-t/\tau_2}$$

Let $v_{B_2}(T_1) = V_0 \Rightarrow T_1 = \tau_2 \ln \dfrac{(2V_s-V_0)}{V_s-V_0} \approx 0.7\tau_2$

$v_{c2}(T_1) = v_{B2}(T_1) = V_o$ $\qquad$ $v_{c1}(T_1) = -V_s+V_o$ (Since $\tau_1 \ll \tau_2$, v_{02} has reached to V_s)

At $t = T_1$ regenerative switching occurs and T_1 becomes OFF T_2 becomes SAT. We have the model in Fig. 2

From Fig.2:

$v_{B_1}(T_1^+) = v_{c_1}(T) = -V_s+V_o$ $\qquad$ $v_{B2} = V_o$ $\qquad$ $v_{01}(T_1^+) = V_o - v_{c2}(T)$

$v_{B_1}(\infty) = V_s$ $\qquad$ $\tau_3 = R_1C_1$ $\qquad$ $v_{02} = 0$ $\qquad$ $= 0$

$v_{B_1}(t) = V_s+(-2V_s+V_o)e^{-(t-T_1)/\tau_3}$ $\qquad$ $v_{01}(\infty) = V_s$

$\tau_4 = R_{L_1}C_2$

Usually $\qquad \tau_4 \ll \tau_3$

Let $v_{B_1}(T_2) = V_o$ ∴ at $t=T_2$ we have regenerative switching

$v_{B_1}(T_2) = V_o = V_s+(-2V_s+V_o)e^{-(T_2-T_1)/\tau_3}$ $\qquad$ T_1 becomes SAT
T_2 becomes OFF.

$$\therefore \quad T_2 = T_1+\tau_3 \ln \frac{2V_s-V_o}{V_s-V_o} \simeq T_1+ 0.7\tau_3$$

Since at $t=T_2$ we have the same conditions as at $t=0$, i.e.

$$v_{B_1}(T_2) = v_{B_1}(0^-) = V_o, \qquad v_{01}(T_2) = v_{01}(0^-) = V_s$$

$$v_{02}(T_2) = v_{02}(0^-) = 0$$

the waveforms will repeat as indicated in the below figure:

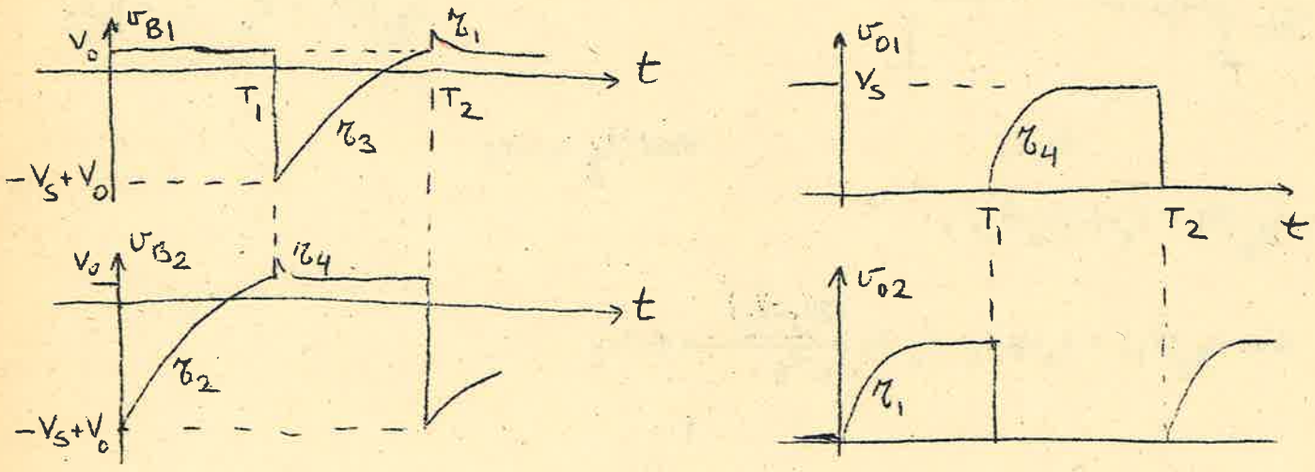


Fig. 4

Loop Gain: Since regenerative switching occurs at a short time interval, the capacitors behave as constant voltage sources. Therefore in loop gain calculation they are short circuits.

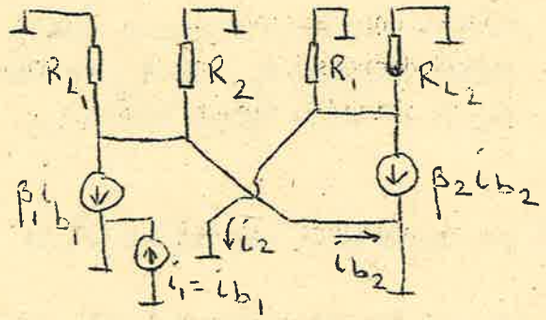


FIG. 5

$$i_2 = -\beta_2 i_{b2} = -\beta_2(-\beta_1 i b_1) = \beta_2\beta_1 i_{b_1}$$

$$\therefore \quad i_2 = \beta_2\beta_1 i_1$$

$$A_L = \frac{di_2}{di_1} = \beta_2\beta_1 > 1$$

As seen from Fig. 4, v_{01} and v_{02} have a certain rise time depending on τ_1 and τ_4. To obtain a sharp rise for v_{01} one can use the below circuit.

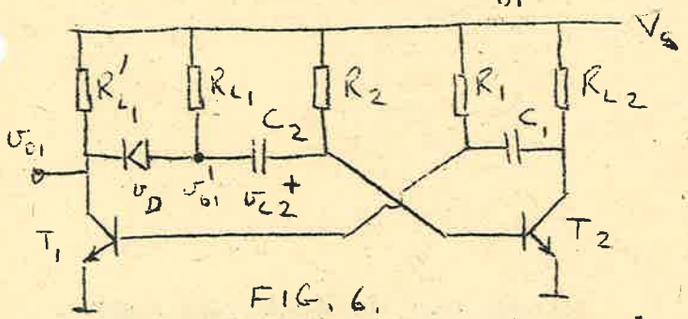


FIG. 6.

When T_1 is SAT and T_2 is OFF, the diode is ON by the currents three R_{L_1} and R_2, C_2. $v_{01} = 0$, $v'_{01} = V_D$. When $v_{02} = V_o - V_D$ we have reg. switching. T_2 becomes SAT T_1 becomes OFF, and diode is OFF because voltage across it is $-v_{c2}+V_o-V_s = V_D-V_s<V_D$.

$\therefore$ v_{01} immediately becomes V_s and v'_{01} and v'_{01} rises to V_s by a time constant $R_{L_1}C_2$

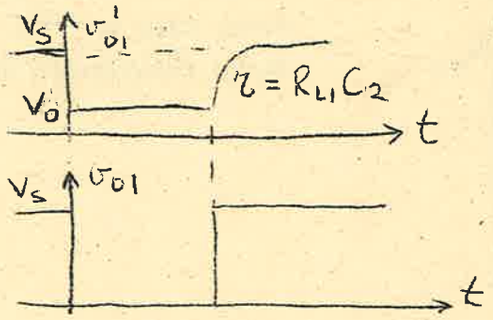


FIG. 7

The standard astable multivibrator circuit, in Fig.1, is said to be self starting. This means that when the supply is turned on periodic square wave waveforms are observed at the collectors of the transistors. But in some cases one may observe zero voltage at both of the collectors (due to improper choice for the resistors R_1, R_2, R_{L_1}, R_{L_2}). In this case both of the transistors are saturated, and since v_{01} and v_{02} are both constant at zero volts, the circuit is at steady state. The equivalent model of the circuit in Fig.1 is then:

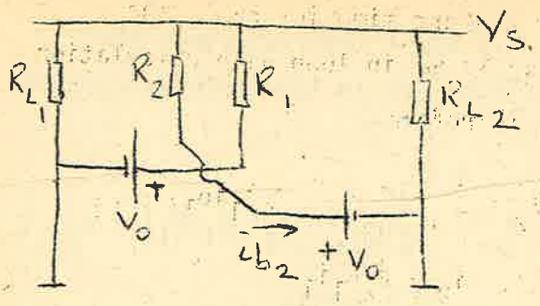


Fig.8

Since the resistors are chosen such that $\beta i_b > i_{cSAT}$, the transistors will remain in SAT mode. To eliminate this failure one can increase R_1 and R_2 or/and decrease R_{L_2} and R_{L_1} so that βi_b is slightly larger than i_{cSAT}.

An astable circuit in which both of the transistors can not be SAT is depicted in Fig.9

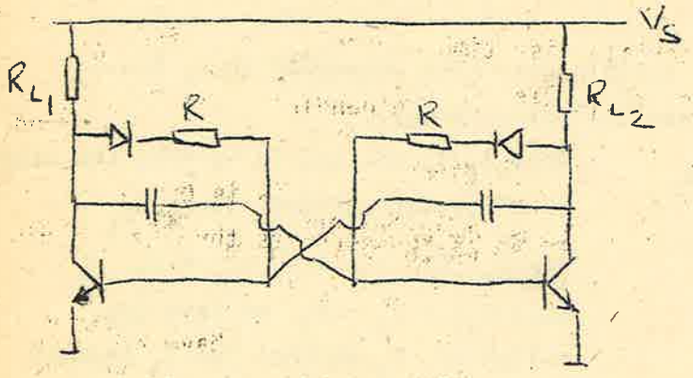


Fig.9

Of both of the transistors are SAT, then the circuit is at steady state and we then have the model in Fig.10

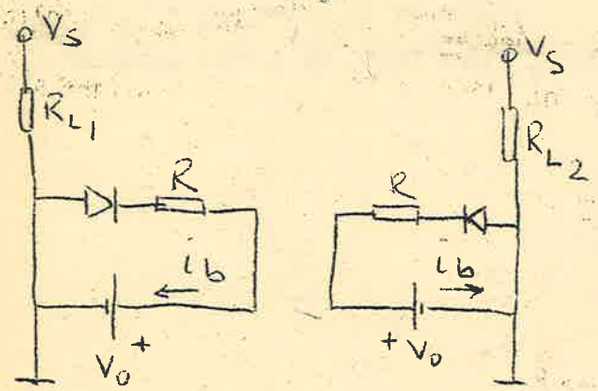
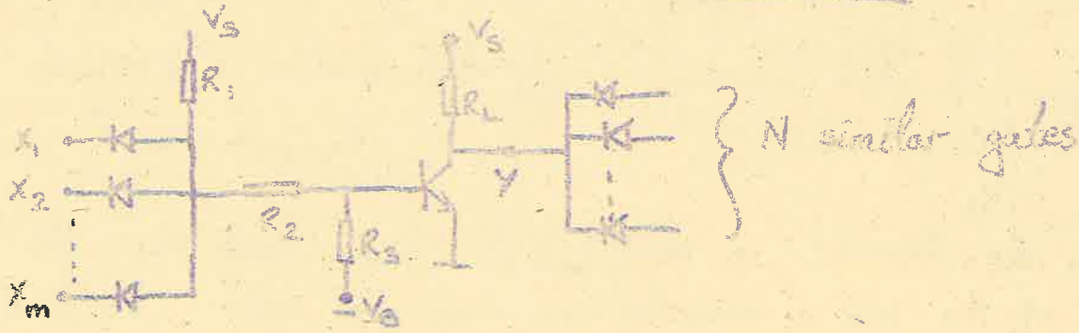


FIG. 10

Observe that the diodes are reverse biased by the voltage sources 'V_o'. Hence they are OFF. Therefore $i_b = 0$. Hence transistors can not be SAT.

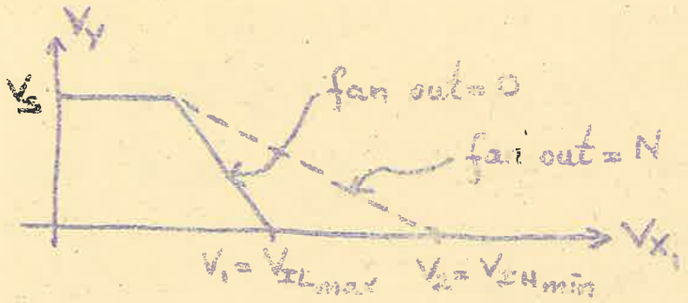
EE 411 SUPPLEMENTARY NOTE

DESIGN EXAMPLE FOR DTL NAND GATE



Obtain v_Y vs. v_{X_1} (since only one diode can conduct at a time, the rest of the input diodes are ignored), by choosing R_1, R_2, R_3, R_L

V_Y vs. V_{X_1} will have the following shape:



Assume the following are specified:

1/ $I_{C\,max}$ (max. collector current). $I_{C\,max}$ is limited due to limitation in power dissipation.

2/ $V_{IL\,max}$ (V_1), $V_{IH\,min}$ (V_2) (these values are determined from noise margin considerations)

3/ Max. fan out = N

4/ R_L (is chosen from dynamic speed considerations).

Design data:

$V_S = 6v$ $\quad V_1 \geq 1.4v.$ $\quad \beta \geq 50$ $\quad V_{CE\,SAT} = 0.4.$

$V_B = 6v$ $\quad V_2 \leq 3.4v.$ $\quad V_0 = 0.6v$ $\quad I_{C\,max} = 10\,mA$

$N = 5$ $\quad V_0 = 0.6v$

$2K \leq R_L \leq 10K$

Given the above design data choose R_1, R_2, R_3.

Solution:

1/ choose $R_L = 4.7K$

2/ Using $I_{c\,max}$, N, R_L determine R_1:

$$I_{c\,SAT} = \frac{V_{cc}}{R_L} + NI_b \leq I_{c\,max} = 10mA$$

$$\frac{6}{4.7} + NI_b \leq 10 \Rightarrow I_b \leq 1.85mA$$

$$\therefore I_{b\,max} = 1.75mA$$

When the transistor is SAT (i.e. $V_b = 0$) we know that the transistors of the gate connected as load are OFF. $\therefore$ we have:

$$I_b = \frac{V_x - V_b}{R_1} = \frac{V_{cc} + V_{BB}}{R_2 + R_3} \leq I_{b\,max} = 1.75mA$$

$$\frac{5.4}{R_1} - \frac{6.6}{R_2 + R_3} \leq 1.75mA \quad (1)$$

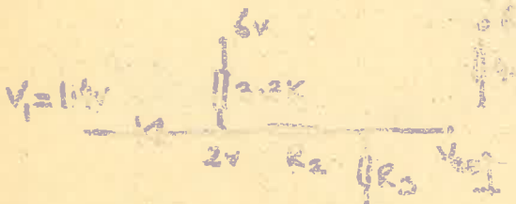
Assume R_1, R_2 and R_3 satisfy: $R_1 \ll R_2 + R_3$ (2)

Then from eqn. (1) we have $\frac{5.4}{R_1} \leq 1.75 \Rightarrow R_1 \geq 3.09K$.

Choose $\boxed{R_1 = 3.3K\Omega}$. Then $I_b = \frac{V_{cc} - V_b}{R_1} = \frac{5.4}{3.3} = 1.64mA$ (3)

3/ For $V_{x_1} \leq V_1$, TR must be OFF.

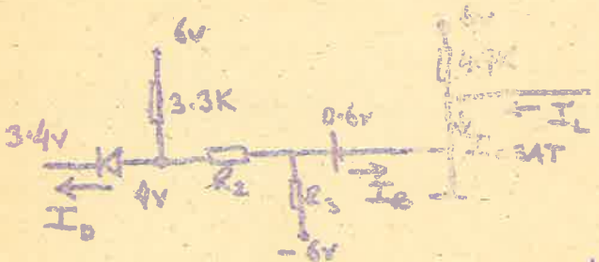
Assume that for $V_{x_1} = V_1$ TR is OFF



$$V_{BE} = \frac{2}{R_2 + R_3} R_3 - 6 \leq V_b = 0.6v$$

$$\boxed{R_2 \geq 0.61 R_3} \quad (4)$$

4/ For $V_{x_1} \geq V_2$ TR must be SAT. Worst case occurs for $V_{x_1} = V_2$



$$I_{c\,SAT} = I_L - \frac{6}{4.7} = NI_b + \frac{6}{4.7}$$

Substituting (3) we obtain

$$I_{c\,SAT} = 5(1.64) + \frac{6}{4.7} = 9.5mA$$

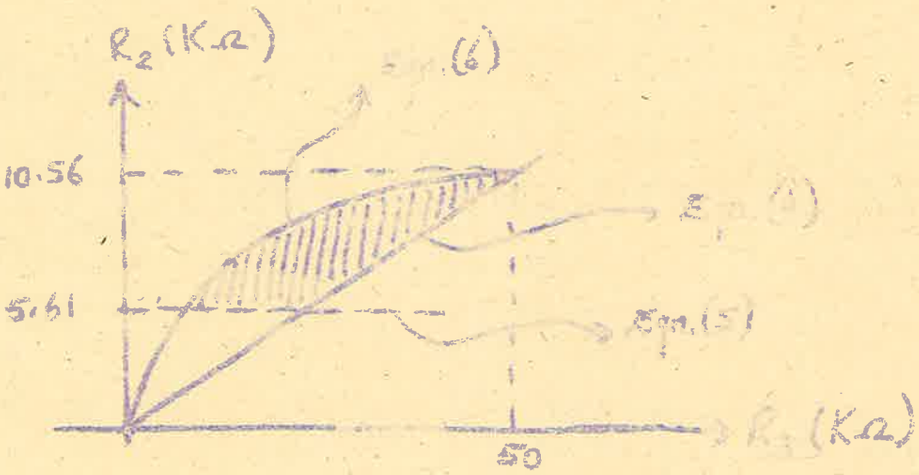
Assume that D is required to be on (otherwise the input can't control the circuit), i.e. $I_b > 0$

$I_D = \frac{2}{20} - \frac{0.1}{R_2} > 0 \Rightarrow$ [illegible] (5)

To make the TR SAT. $\beta_{min} I_B > I_{CSAT} = 9.5mA$

$$I_B = \frac{3.4}{R_2} - \frac{6.6}{R_3} > \frac{9.5}{\beta_{min}} = \frac{9.5}{50} \rightarrow \boxed{R_2 < \frac{3.4}{0.19 + \frac{6.6}{R_3}}} \quad (6)$$

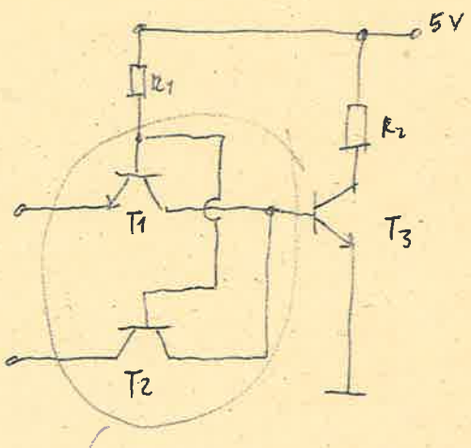
Using equations (1), (5) and (6) we obtain:



The shaded area is the feasible region.

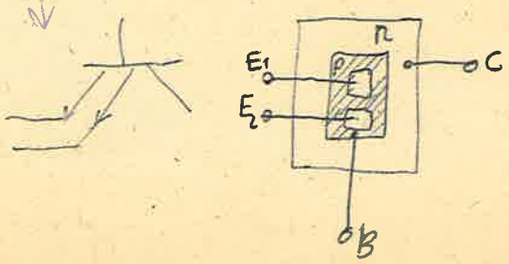
After choosing R_2 and R_3 from the feasible region, be sure that inequality (2) is satisfied.

NAND TTL Vgate:



A	B	T_1	T_2	T_3	V_o
L	L	SAT	SAT	OFF	H
L	H	SAT	REVACT	OFF	H
H	L	REV.	SAT	OFF	H
H	H	REVACT	REVSAT	SAT	L

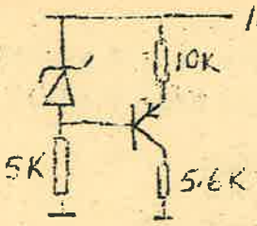
NAND Gate.



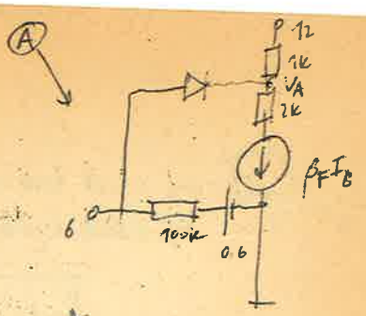
EE 442

Exercises

(1) Find the state of the transistor. $V_\gamma = 0.6v$, $V_Z = 5v$, $\beta_F = 50$.



Ans: T1 ACT



Assume D is OFF:

$I_B > 0.05mA$

$\beta_F I_B = 2.7mA$.

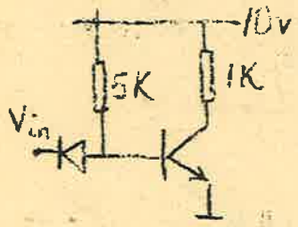
$V_A = 12 - (1k)(2.7mA)$

$= 9.3\ V.$

$V_D = 6 - 9.3 = -3.3V < 0$

D is OFF

(2) Find the states of the diode and of the transistor for



a) $V_{in} = -2v$

b) $V_{in} = 5v$

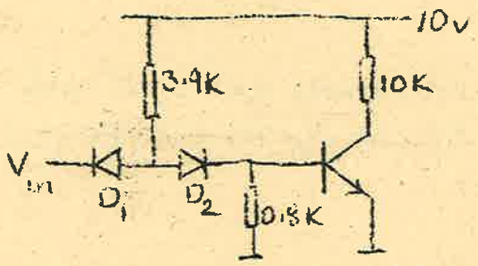
Ans: a) D on, Tr off

b) D off, Tr sat

$V_\gamma = 0.6v$, $V_D = 0.6v$, $\beta_F = 50$

(3) Find the states of the diodes and of the transistor for

a) $V_{in} = 5v$ b) $V_{in} = -2v$

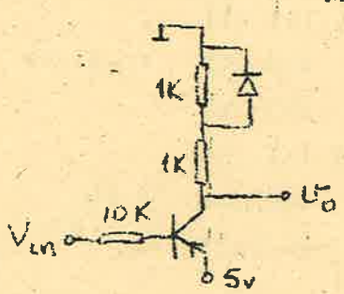


Ans: a) D_1 off, D_2 on, Tr sat

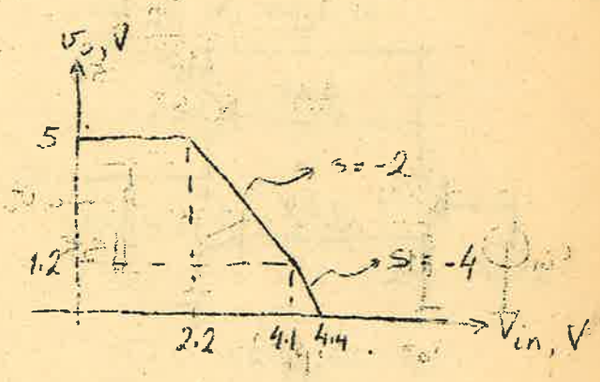
b) D_1 on, D_2 off, Tr off

$V_\gamma = 0.6v$, $V_D = 0.6v$, $\beta_F = 50$

(4) Find V_o vs. V_{in} for $0 \leq V_{in} \leq 10v$.



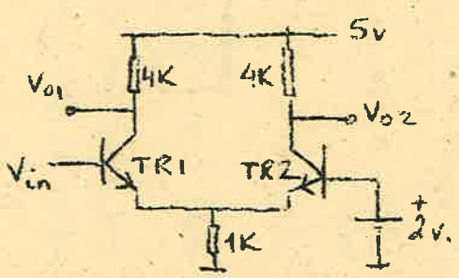
Ans:



$V_\gamma = 0.6v$, $V_D = 0.6v$, $\beta_F = 20$

(5) Find the states of the transistors and V_{o1} and V_{o2} for

a) $V_{in} = 0$ b) $V_{in} = 4v$



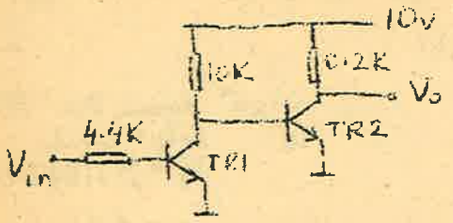
Ans: a) Tr1 off, Tr2 sat, $V_{o1} = 5v$, $V_{o2} = 1.4v$

b) Tr1 sat, Tr2 off, $V_{o1} = 3.4v$, $V_{o2} = 5v$

$V_\gamma = 0.6v$, $\beta_F = 100$

(6) a) Find the states of the transistors and V_o for i) $V_{in}=0$ ii) $V_{in}=5v$

b) Find V_o vs. V_{in} for $0 \leq V \leq 5v$

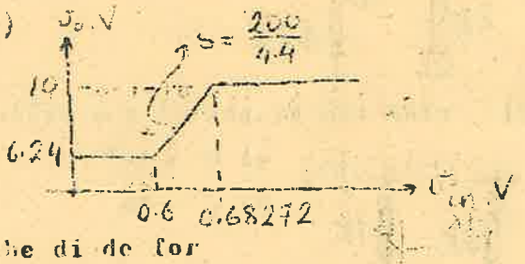


$\beta_{F_1}=50, \beta_{F_2}=20, V_o=0.6v$

Ans: a) i) Tr1 Off, Tr2 Act, V = 0.24v

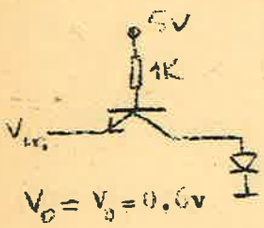
ii) Tr1 Sat, Tr2 Off, V = 10v

b)



(7) Find the states of the transistor and of the diode for

a) $V_{in}=4v$ b) $V_{in}=0.2v$



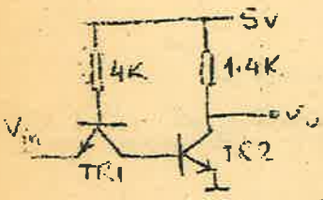
$V_o = V_\gamma = 0.6v$

Ans: a) Tr Revact, D on

b) Tr Sat, D off

(8) Find the states of the transistors and V_o for

a) $V_{in}=4v$ b) $V_{in}=0.2v$



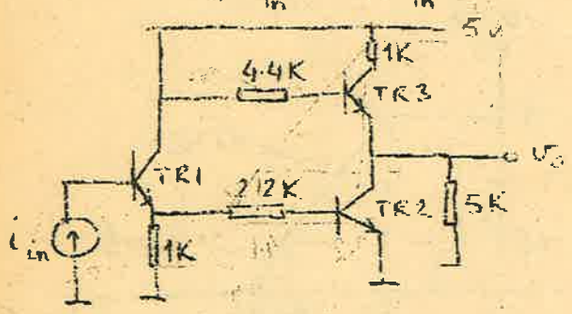
$\beta_R=0.02, \beta_F=10, V_\gamma=0.6v$

Ans: a) Tr1 Revact, $V_o=0$, Tr2 Sat

b) Tr1 Sat, $V_o=5v$, Tr2 off

(10) Find the states of the transistors and V_o for

a) $i_{in}=0$ b) $i_{in}=1mA$



$V_\gamma=0.6v, \beta_F=10$

Ans: a) Tr1 Off

Tr2 Off $V = 4.20v$

Tr3 Act

b) Tr1 Sat

Tr2 Sat $V = 0$

Tr3 Sat

Remove Tr:

Find the state of D:

Assuming D is OFF:

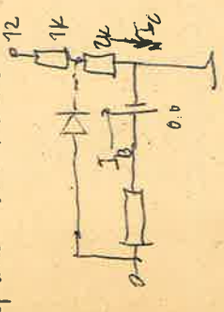
$V_D = 6-12 = -6$ ✓ D is OFF.

$V_{BE} = 6V$, T must OFF.

$V_{BC} = -6$ V.

$V_{BE} > V_{BC}$ Tr SAT or ACT

Replace SAT model:



Again find the state of Tr.

Assume Dis OFF:

$6 - \frac{12}{3}\times 2 = -2V < 0$ ✓ Dis OFF.

$I_B = \frac{6-0.6}{100K} = 0.054\ mA.$

$I_C = \frac{12}{3K} = 4\ mA.$

$\beta_F I_B = 2.7 < 4$ Tr ACT

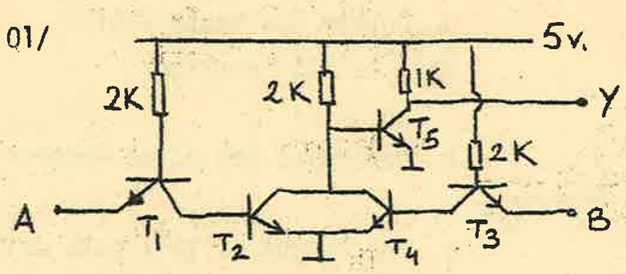
We must find again state of D because when we were finding the state of diode we have assumed that Tr is SAT

(A)

EE 411

Exercise

Q1/

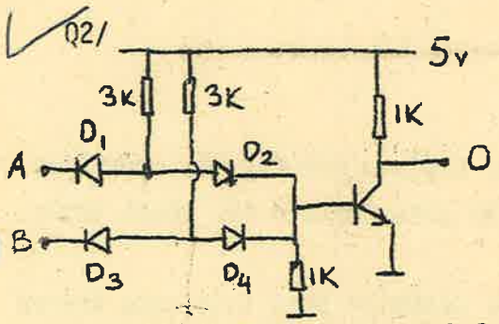


$\beta = 20$, $\beta_R = 0.02$, $V_o = 0.6v$.

a) Find the truth table showing the states of the transistors. Take $V_{IH} = 2^v$, $V_{IL} = 0.2v$.

b. Assuming that this gate drives similar gates determine the max. fan-out.

Q2/



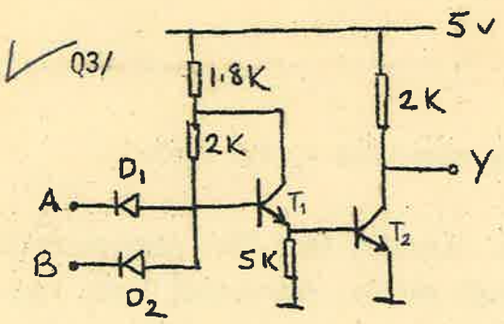
$\beta_F = 30$, $V_o = 0.6v$, $V_D = 0.6v$.

a. With $V_{OH} = 5v$, $V_{OL} = 0v$. explain the operation of the gate. Obtain the truth table. What is its function?

b. What are the noise margins?

c. Assuming that it drives similar gates what is the max. fan-out. (consider the worst case input conditions)

Q3/



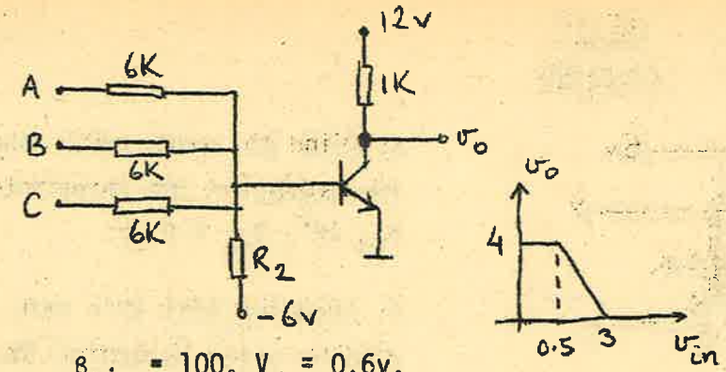
$\beta_F = 30$, $V_o = V_D = 0.6v$.

NAND a. Obtain the truth table. What is its function?

b. When the inputs of this gate are obtained from the outputs of similar gates, calculate the max. fan-out.

c. Calculate the noise margins under worst case loading conditions.

Q4/



β_{min} = 100, V_γ = 0.6v.

An RTL gate and its worst case transfer characteristic is given.

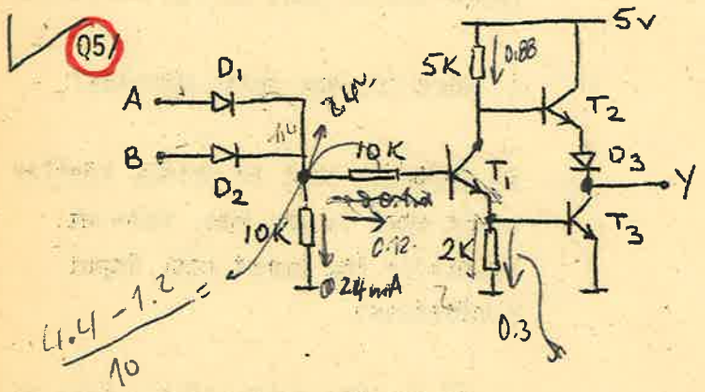
a. Obtain the truth table. What is its function?

b. Determine the noise margins.

c. The output of this gate drives similar gates. Calculate the max. fan-out. (14)

d. Determine the permissible regions of R_2.

Q5/



β_F = 20, V_o = 0.6v, V_D = 0.6v.

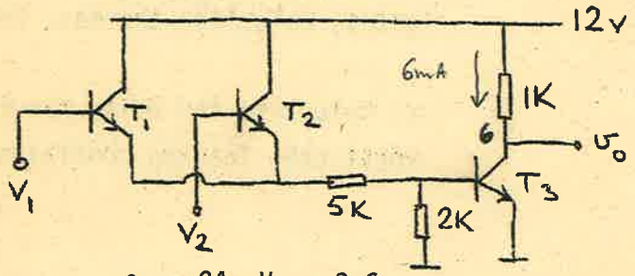
NOK a. Explain briefly the operation of the gate. Obtain the truth table.

b. Assuming that this gate drives similar gates and V_{OHmin} = 2.8v, calculate the max. fan.out (take $V_A = V_B$ = 0v)

13

c. Calculate the max. current that can be sunk by this gate when V_A=3v, V_B=2v.

Q6/



β_F = 24, V_o = 0.6v.

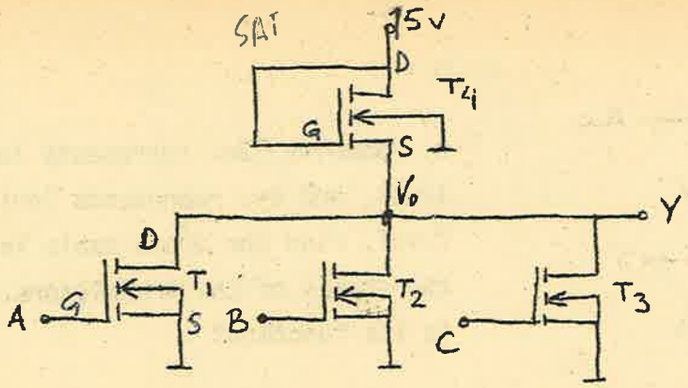
NOK a. Assuming that 10v. represents logic high and 0v. represents logic low, give the truth table. What is its function?

b. Find v_o vs. V_1 with V_2 grounded,

c. Calculate the max. fan-out for $V_{OH_{min}}$ = 6v.

156

Q7/



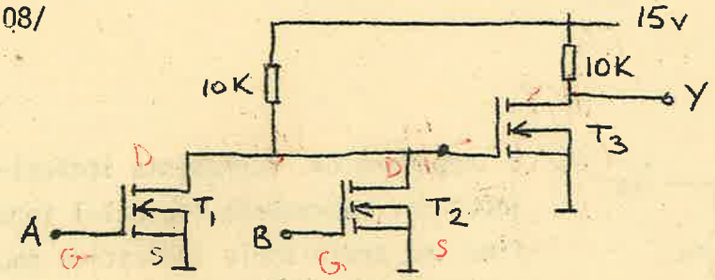
a. Find the truth table.

b. What is V_{YH}? Obtain $V_{Y_{L_{min}}}$ and $V_{Y_{L_{max}}}$.

For T_4: K_n=0.02 mA/V^2, V_{T_n} = 3v

For T_1,T_2,T_3: K_n=0.2mA/V^2 , V_{T_n}= 5v

Q8/



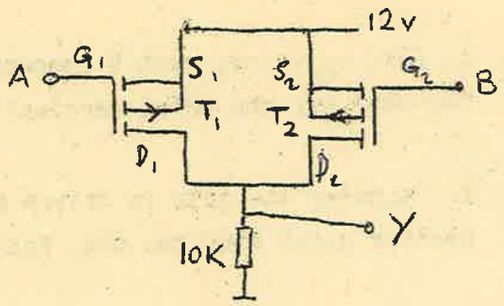
V_{T_n} = 5v, K_n = 0.2 mA/V^2

Assuming this gate is driven by similar gates:

a. Explain the operation qualitatively and give the truth table. What is its function?

b. Find V_{YH} and V_{YL}.

Q9/

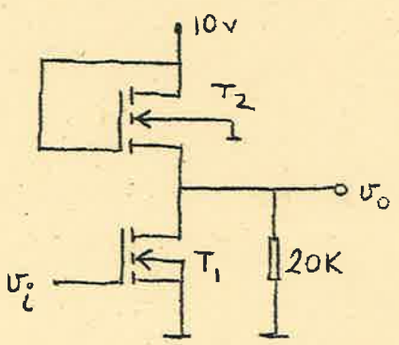


K_p = 0.2 mA/V^2 , V_{T_p} = 6v.

a. Find the truth table. What is its function?

b. Assuming that the gate is driven by similar gates find V_{YL}, $V_{YH_{min}}$ and $V_{YH_{max}}$.

Q10/



$V_{T_{n_1}}$ = 5v $V_{T_{n_2}}$ = 2v

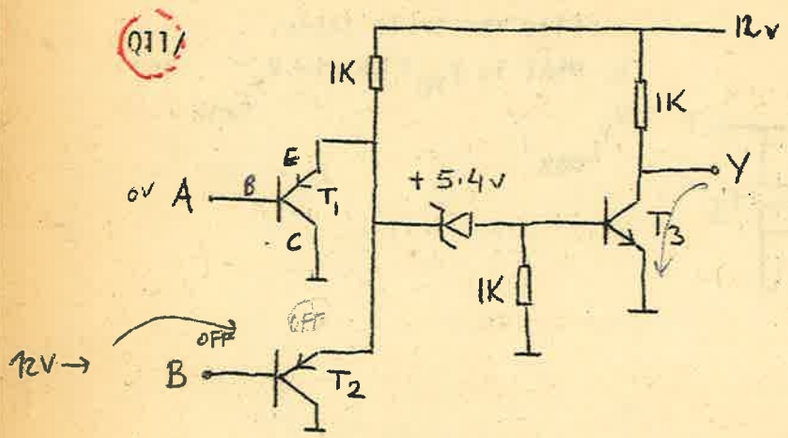
K_{n_1} = 0.8 mA/V^2 K_{n_2} = 0.1 mA/V^2

For the given MOSFET inverter find v_o and the states of the transistors for

a. v_i = 2v

b. v_i = 10v

Q11/



V_0 = 0.6 v

$\beta_1 = \beta_2 = 3$

$\beta_3 = 20$

NAND

(4)

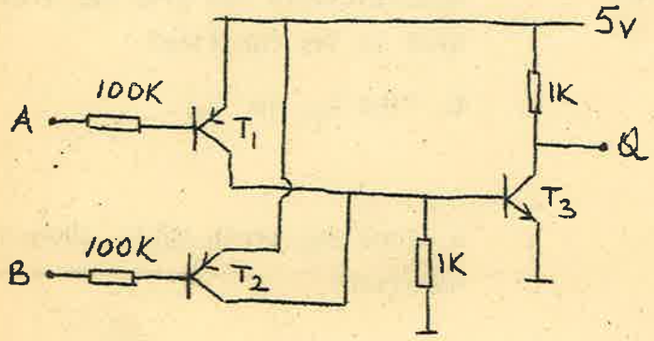
a. Assuming 12v. represents logical-1 level, and 0v. represents logical-0 level, find the truth table indicating the states of the transistors. What is its function?

b. With T_2 OFF find V_Y vs. V_A and find the noise margins.

(33)

c. Find the max. fan-out.

Q12/



β= 50, V_0 = 0.6v.

AND

a. Assuming 0v. represents logical-0 input, 5v. represents logical-1 input, find the truth table indicating the states of the transistors. What is its function?

b. Find v_Q vs. v_A with B connected to 5v. What are the noise margins?

c. Assuming the gate is driven by similar gates find the max. fan-out.

ANSWERS

Q1/ a)

A	B	T_1	T_3	T_2	T_4	T_5	Y
L	L	SAT	SAT	OFF	OFF	SAT	L
L	H	SAT	RACT	"	SAT	OFF	H
H	L	RACT	SAT	SAT	OFF	"	H
H	H	"	RACT	"	SAT	"	H

⇒ PLC OR Gate

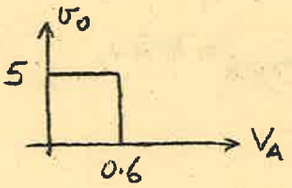
b) Max. fan-out = 18

Q2/ a)

A	B	D_1	D_2	D_3	D_4	T	O
L	L	ON	OFF	ON	OFF	OFF	H
L	H	"	"	OFF	ON	SAT	L
H	L	OFF	ON	ON	OFF	"	L
H	H	"	"	OFF	ON	"	L

⇒ PLC NOR Gate

b)



LNM = 0.6v

HNM = 4.4v

c) Max. fan-out = 10

Q3/ a) PLC-NAND Gate b) Max. fan-out = 47 c) LNM = 0.6v HNM = 4.4v

Q4/ a) PLC-NOR Gate b) LNM = 0.5v HNM = 1v c) Max. fan-out = 12

74?

d) $15.8K < R_2 < 24K$

Q5/ a)

A	B	D_1	D_2	T_1	T_2	T_3	D_3	Y
L	L	OFF	OFF	OFF	ACT	OFF	ON	H
L	H	"	ON	SAT	OFF	SAT	OFF	L
H	L	ON	OFF	"	"	"	"	L
H	H	Diode with highest input is ON		"	"	"	"	L

⇒ PLC-NOR Gate.

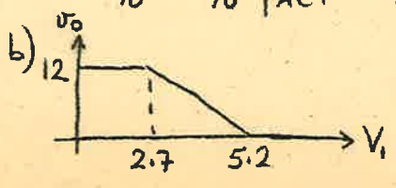
b) Max. fan-out = 13 c) Max. current that can be sunk = 14mA

Q6/ a)

V_1	V_2	T_1	T_2	T_3	V_o
0	0	OFF	OFF	OFF	12
10	0	ACT	"	SAT	0
0	10	OFF	ACT	"	0
10	10	ACT	"	"	0

⇒ PLC NOR-Gate

b)



c) Max-fan out = 156

Q7/ a)

A	B	C	T_1	T_2	T_3	Y
L	L	L	O	O	O	H
L	L	H	O	O	N	L
L	H	L	O	N	O	
L	H	H	O	N	N	
H	L	L	N	O	O	
H	L	H	N	O	N	
H	H	L	N	N	O	
H	H	H	N	N	N	L

O : OFF
N : N

⇒ PLC NOR gate

b) $V_{YH} = 12\,v$ $V_{YL\,min} = 0.33\,v$ $V_{YL\,max} = 0.94\,v$

Q8/ a)

A	B	T_1	T_2	T_3	Y
L	L	OFF	OFF	NSAT	L
L	H	//	ON	OFF	H
H	L	ON	OFF	//	H
H	H	//	ON	//	H

⇒ PLC OR Gate

b) $V_{YH} = 15\,v$
$V_{YL} = 0.74\,v$

Q9/

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

⇒ PLC NAND Gate

b) $V_{YL} = 0.$ $V_{YH\,min} = 11\,v.$ $V_{YH\,max} = 11.5\,v.$

Q10/ a) $v_o \simeq 5.63\,v$ T_1 OFF, T_2 SAT

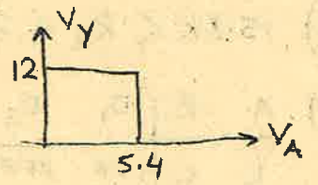
b) $v_o \simeq 0.71\,v$ T_1 NSAT, T_2 SAT

Q11/ a)

A	B	T_1	T_2	T_3	Y
L	L	ACT	ACT	OFF	H
L	H	//	OFF	//	H
H	L	OFF	ACT	//	H
H	H	//	OFF	SAT	L

⇒ PLC NAND gate

b)



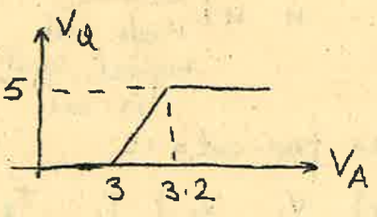
c) $HNM = 12 - 5.4 = 6.6\,v$
$LNM = 5.4\,v.$

Q12/ a)

A	B	T_1	T_2	T_3	Q
L	L	ACT	ACT	SAT	L
L	H	//	OFF	//	L
H	L	OFF	ACT	//	L
H	H	//	OFF	OFF	H

⇒ PLC AND Gate

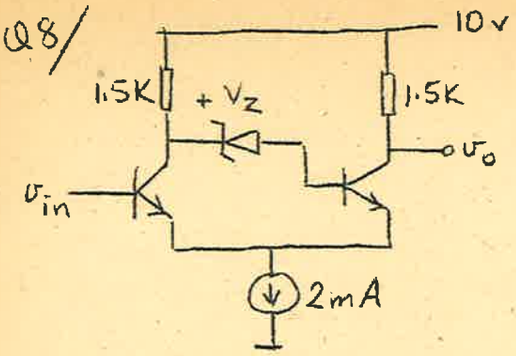
b)



$LNM = 3\,v$ $HNM = 1.8\,v$

c) $N = 1704$

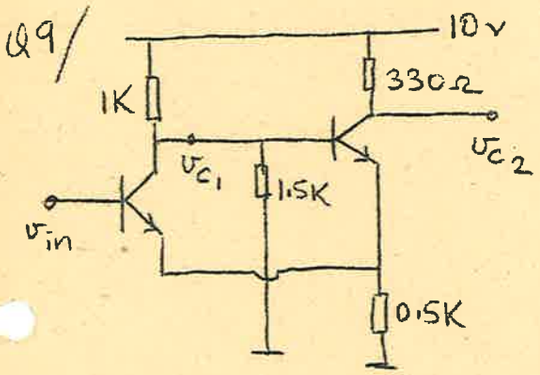
Q8/



Find the transfer characteristic v_o vs. v_{in} for $0 < v_{in} < 10v$.

$\beta = 100$, $V_o = 0.6v$, $V_Z = 5v$

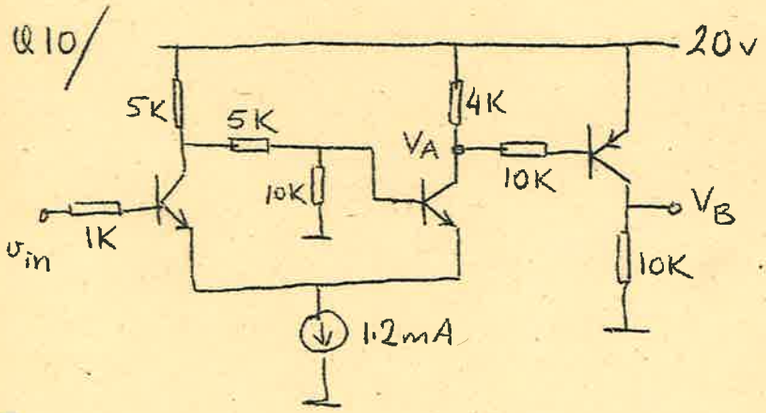
Q9/



Plot v_{C_1} and v_{C_2} vs. v_{in} for $0 \le v_{in} \le 10$

$\beta = 100$, $V_o = 0.6v$

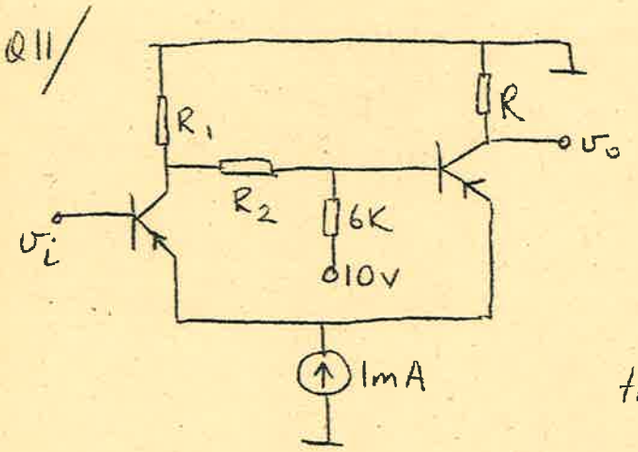
Q10/

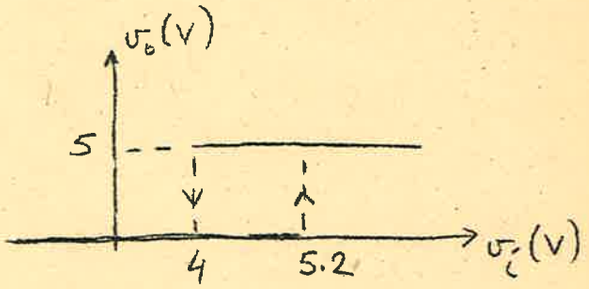


Find and plot V_A and V_B vs. v_{in}

$\beta = 100$, $V_o = 0.6v$

Q11/





Determine R, R_1 and R_2 so that the above characteristic is obtained.

$\beta = 50$, $V_o = 0.6v$